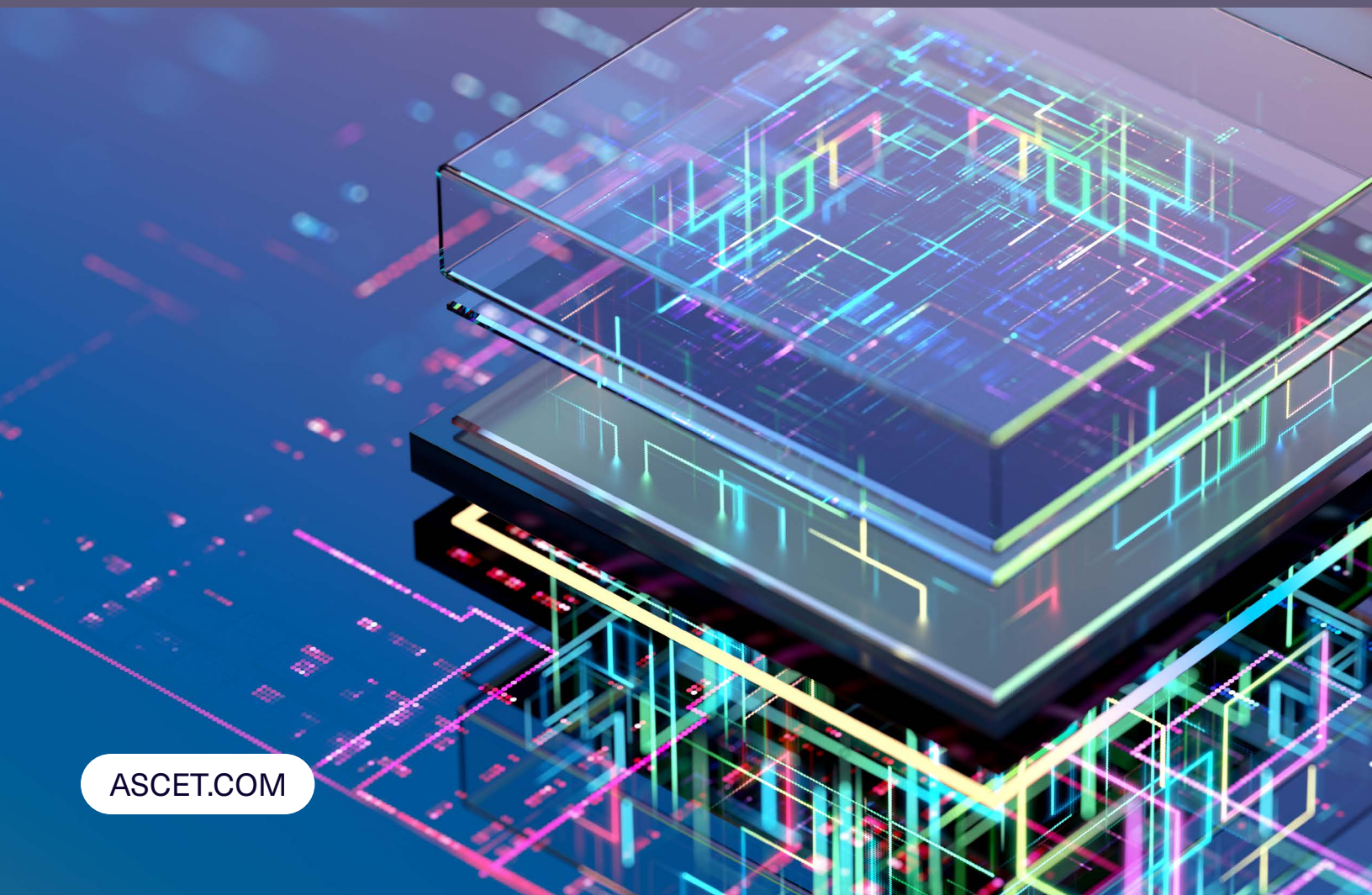
ASCET
CENTER OF EXCELLENCE

ADVANCING STANDARDIZATION FOR
CRITICAL AND EMERGING TECHNOLOGIES

Standardization Environmental Scan: Semiconductors & Microelectronics



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Purpose and Methodology of the Environmental Scan

This standardization environmental scan serves as a foundational step in understanding the current state of standardization for semiconductors and microelectronics as critical and emerging technologies (CETs). It is intended to identify existing standards, key stakeholders, strategic documents, and emerging gaps to inform future activities such as CET-specific workshops, roadmap development, and prioritization of standardization efforts. The assessment supports ASCET's broader goal of aligning standardization with national competitiveness, economic security, and innovation priorities.

This preliminary assessment draws on a targeted synthesis of publicly available standards databases; government and industry strategic documents; and stakeholder inputs from government, industry, and academia. The scope was intentionally constrained to focus on standards and initiatives with significant relevance to U.S. leadership in semiconductors and microelectronics, including those developed or influenced by U.S.-based organizations or international bodies with U.S. participation. This scan represents a point-in-time assessment and may be revisited as priorities and standards evolve.

This assessment goes beyond cataloging existing standards by examining the critical pre-standardization ecosystem including the activities that create the technical foundation for future standards. These efforts include developing interoperable design rules, validating advanced packaging processes, and establishing secure supply chain protocols. Work in areas such as chiplet integration, heterogeneous packaging, and sustainability metrics often begins as collaborative research or pilot programs before formal specifications emerge. By analyzing both explicit contributions (e.g., published draft standards, participation in standards developing organizations [SDOs]) and implicit enablers like shared testbeds, reference architectures, and metrology frameworks, this scan highlights how today's research and development (R&D) initiatives are shaping tomorrow's standards. Understanding these linkages ensures that ASCET and its partners can prioritize actions that accelerate interoperability, reliability, and global harmonization across the semiconductor lifecycle.

CET: Semiconductors & Microelectronics

Semiconductors are materials that conduct electricity under certain conditions; they are essential for modern electronics. Unlike metals, which always conduct, or insulators, which block current, semiconductors can switch between these states. Their conductivity depends on the energy bandgap, which can be adjusted through a process called doping—adding tiny amounts of other elements to change electrical behavior.

Semiconductors power nearly every technology we use, from smartphones and cars to renewable energy systems and high-speed communications. They are critical to economic growth and national security because they enable computing, sensing, and power conversion at scale.

COMMON SEMICONDUCTOR MATERIALS INCLUDE:

- **Silicon (Si):** The most widely used material for chips and integrated circuits (ICs) thanks to its abundance and mature manufacturing processes.
- **Gallium Arsenide (GaAs):** Ideal for high-frequency applications like wireless and satellite systems; also used in LEDs and laser diodes.
- **Silicon Carbide (SiC):** Handles high temperatures and voltages, making it perfect for electric vehicles (EVs) and industrial power electronics.
- **Gallium Nitride (GaN):** Known for efficiency and high-frequency performance; used in power adapters, 5G base stations, and LED lighting.
- **Germanium (Ge):** Offers high electron mobility for specialized uses like infrared optics and high-speed electronics.

SEMICONDUCTORS CAN ALSO BE CLASSIFIED BY DOPING:

- **N-type:** Extra electrons are added, making electrons the main charge carriers.
- **P-type:** Creates “holes” (missing electrons), making holes the main carriers.
- **Intrinsic:** Pure, undoped material, rarely used because it conducts poorly.

BY FUNCTION, CHIPS INCLUDE:

- **Logic chips** for processing instructions in computers and smartphones.
- **Memory chips** for storing data, from dynamic random-access memory (DRAM) to flash storage.
- **Analog and mixed-signal chips** for sensors and power management.
- **Power semiconductors** for controlling electricity in vehicles and energy systems.
- **Optoelectronic devices** like LEDs and photodetectors for lighting and fiber optics.

Semiconductors also come as discrete components (like transistors and diodes) or as ICs, which pack millions or billions of transistors onto a single chip. However, as designs become even more complex, the industry is shifting toward a new architectural model: chiplets. Instead of forcing all functions onto one giant piece

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of silicon, this modular approach breaks a chip into smaller, specialized building blocks that are "stitched" together in a single package, allowing engineers to mix and match different materials and manufacturing nodes. This significantly boosts performance while reducing the cost and complexity of high-end processors.

Current State of the CET Topic: Semiconductors & Microelectronics

Semiconductors and microelectronics are the "backbone" of the digital economy; hundreds of billions of chips power consumer devices, industrial systems, and government infrastructure worldwide. Industry forecasts project the market will surpass $1 trillion by 2030 due to structural demand from artificial intelligence (AI) accelerators, high-bandwidth memory (HBM), and advanced interconnects. AI infrastructure buildouts are driving major changes in compute, memory, networking, and storage; this has led to a major "giga cycle" in chip demand. Beyond AI, applications including automotive, telecommunications, and industrial automation are using more chips than ever before, leading to greater overall demand and raising the strategic importance of a resilient, stable chip supply for both commercial and public sectors.[1, 2, 3, 4, 5]

The United States is still a leader in chip design and overall industry revenue despite a drop in its share of global chip manufacturing from 37% in 1990 to about 10% in 2022. This drop has pushed the country to rebuild domestic production for advanced chips and packaging. The CHIPS and Science Act sets aside about $52.7 billion for incentives, research, and workforce programs, including $39 billion for building new factories. These funds come through grants, loans, and tax credits to encourage private companies to invest. Since the law passed, companies have announced nearly $400 billion in U.S. semiconductor and electronics projects. Federal agreements already include more than $30 billion in direct funding and $25 billion in loans, with a goal of raising U.S. production of advanced chips to about 30% of global supply by 2032. These investments focus on expanding capacity for logic, memory, and advanced packaging; however, Asia still dominates chip manufacturing and equipment spending, which keeps global supply chains exposed to geopolitical and shipping risks.[6, 7, 8, 9]

AI chips and custom processors are growing fast as big tech companies and governments build larger systems and move AI closer to the edge. HBM is a major bottleneck; revenue is expected to jump from about $16 billion in 2024 to more than $100 billion by 2030 due to the need for faster data transfer in AI workloads. Meanwhile, advanced packaging (including chiplets and 3D integration) has shifted more value to assembly and testing. Companies are adopting optical and high-speed interconnects to keep performance high and energy use low. This includes co-packaged optics and new network designs for moving data more efficiently in large AI systems.[10, 11, 12, 13]

Workforce and security rules are critical to U.S. leadership in semiconductors. Federal funding is tied to training programs to fill jobs in chip manufacturing, packaging, and equipment maintenance. Companies that receive funding must

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follow national security rules, including a 10-year ban on expanding advanced chip production in certain foreign countries to protect U.S. interests and supply chain security. These public and private investments are expected to greatly increase U.S. chip and packaging capacity through the early 2030s. The global market is pushing toward $1 trillion by 2030 due to AI growth and increased use of chips in cars, telecom, and industry.[14, 15, 16, 17]

Standards Overview

Establishing standards for semiconductors and microelectronics is critical because these technologies are used everywhere—from consumer electronics to defense systems. Standards help ensure chips are reliable, safe, and can work together across different devices and systems. Unlike emerging fields like quantum, semiconductor standards are mature in many areas, but new challenges are appearing as technology advances.[18, 19]

Different parts of the semiconductor industry need different standards. For example, chip design and testing follow Institute of Electrical and Electronics Engineers (IEEE) and Joint Electron Device Engineering Council (JEDEC) specifications, while manufacturing processes rely on SEMI and International Organization for Standardization (ISO) standards for wafer handling, materials, and quality control. Automotive chips must meet functional safety standards like ISO 26262; strict rules exist for electrostatic discharge (ESD) and electromagnetic compatibility (EMC) to prevent failures. Security standards are also growing in importance as chips become central to critical infrastructure.[20, 21, 22]

Some areas are well covered, but others—such as advanced packaging, chiplets, and heterogeneous integration—still lack complete standards. Industry groups and government agencies, including the National Institute of Standards and Technology (NIST) CHIPS R&D office, are working on new frameworks for supply chain trust, traceability, and data interoperability to improve security and transparency. Global cooperation is also a priority, with U.S. and EU initiatives focused on aligning standards internationally to avoid fragmentation and trade barriers.[23, 24, 25, 26]

Overall, semiconductor standards are more developed than those for quantum technologies, but rapid changes in AI hardware, packaging, and security mean new standards will be needed to keep pace with innovation.

STAKEHOLDERS

The stakeholders listed in the following table represent major players in the semiconductor and microelectronics ecosystem as well as “ASCET-aligned collaborators”—companies that actively engage with ASCET-aligned standards groups, workshops, and consortia to advance standards for CETs. These organizations influence global supply chains and technical progress across logic, memory, packaging, and advanced materials. Their collective impact is evident in industry trends: the semiconductor market is projected to reach $1 trillion by 2030, driven by surging demand for AI chips and advanced packaging technologies—a

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trajectory that underscores the strategic importance of these stakeholders in shaping future standards and ensuring interoperability.[27,28]

Disclaimer: The following table is based on public information only. Listed companies may have different roles within biotechnology or standardization than described. This table is not exhaustive and may not include some major contributors to semiconductor and microelectronic standardization.

Advanced Micro Devices (AMD) [29, 30, 31`, 32, 33, 34, 35, 36, 37, 38, 39]

Role in CET
In 2025, AMD unveiled a new series of semiconductors for AI-enabled business laptops and desktops. This series forms part of AMD's strategy to expand their "AI PC" market share. In 2024, the company's shares had already increased by 14%, which demonstrates significant growth in their AI chip sales. AMD reported $34.6 billion in total revenue for 2025, a 34% increase from the previous year driven largely by chip sales for data center and gaming and client segments.

Role in Standardization of CET
AMD participates in key semiconductor standards bodies such as JEDEC and the Responsible Business Alliance (RBA), working with customers and suppliers to comply with industry standards including Restriction of Hazardous Substances (RoHS) and Registration, Evaluation, Authorization, and Restriction of Chemicals (REACH). AMD's standards engagement supports quality, reliability, and sustainability in semiconductor manufacturing aligned with ASCET's goals.

Applied Materials [40, 41, 42, 43, 44, 45]

Role in CET
Applied Materials is a global leader in semiconductor manufacturing equipment; they offer essential tools for chip fabrication such as thin film deposition, etching, ion implantation, and metrology. Their technologies enhance chip power efficiency, thermal management, throughput, and cost-effectiveness. Applied Materials has major U.S. facilities including Austin, Texas. They are also making strategic investments to expand domestic capacity and are aligned with national goals to strengthen semiconductor supply chains and reduce foreign dependence.

Role in Standardization of CET
Applied Materials plays an active role in semiconductor standards through participation in key consortia like SEMI and the Semiconductor Climate Consortium (SCC). They contribute to developing sustainability standards addressing greenhouse gas emissions, water use, and chemical management. The company also collaborates with NIST and SEMI's Semiconductor Manufacturing Cybersecurity Consortium (SMCC) to advance cybersecurity standards for fabrication facilities and equipment. Their engagement extends to promoting manufacturing excellence via standards that enhance reliability, interoperability, and supply chain transparency, which aligns with ASCET's mission of driving innovation and resilience in CETs.

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Broadcom [46, 47, 48, 49]

Role in CET
Broadcom is a leading global semiconductor company specializing in infrastructure and connectivity solutions, including chips for 5G, broadband, and data centers. In 2023, Broadcom recorded a revenue of $35.8 billion. In 2024, Apple announced a multi-year, multibillion-dollar agreement with Broadcom to develop Film Bulk Acoustic Resonator (FBAR) filters and other 5G radio frequency components. The deal will support more than 1,100 jobs. [50]

Role in Standardization of CET
Broadcom actively participates in semiconductor and communications standards development through organizations such as IEEE, PCI-SIG, and the Open Compute Project. The company contributes to advancing interoperability and performance standards critical to next-generation semiconductor technologies and connectivity solutions.

Cadence Design Systems [51, 52, 53]

Role in CET
Cadence Design Systems is an American multinational computational software and AI company that specializes in electronic design automation (EDA). The company provides software, hardware, and intellectual property (IP) required to design, test, and manufacture modern microchips, advanced packaging, and complete electronic systems. Cadence also offers molecular modeling and biosimulation software.

Role in Standardization of CET
Cadence plays a meaningful role as a technical contributor to electronics-specific standardization development. Cadence participates in standards committees with both Accellera and IEEE.

Intel [54, 55, 56]

Role in CET
Intel is currently the world's largest manufacturer of central processing units and semiconductors. Intel operates 15 wafer labs across the world. The company expects to invest more than $100 billion over the next five years——with Creating Helpful Incentives to Produce Semiconductors (CHIPS) support—–to expand the capacity and capabilities of its U.S. fabs. These investments are expected to create more than 9,000 new Intel jobs, 19,000 construction jobs, and 58,000 indirect jobs with suppliers and supporting industries.

Role in Standardization of CET
Intel plays a significant role in setting global semiconductor standards; they participate in 250+ standards and industry groups worldwide. These include foundational and emerging technology standards organizations such as IEEE, ISO/International Electrotechnical Commission (IEC), Internet Engineering Task Force (IETF), USB Implementers Forum (USB-IF), China Communications Standards Association (CCSA), European Telecommunications Standards Institute

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(ETSI), European Committee for Standardization and the European Committee for Electrotechnical Standardization (CEN-CENELEC), IEC, and the International Telecommunication Union (ITU). Intel's broad involvement supports interoperability and innovation across global supply chains and aligns with ASCET's mission to advance standards for critical and emerging technologies.

LAM Research [57, 58, 59, 60, 61, 62, 63]

Role in CET
LAM Research is a leading global supplier of wafer fabrication equipment and services critical to semiconductor manufacturing. Their product portfolio includes advanced etching, deposition, and cleaning technologies that enable precise patterning and material processing at the nanoscale. LAM's tools support the production of logic, memory, and advanced packaging chips. The company operates significant manufacturing and R&D facilities in the United States and globally; their goals align with national efforts to strengthen domestic semiconductor supply chains and innovation capacity.

Role in Standardization of CET
LAM Research actively participates in semiconductor standards development through engagement with key industry organizations such as SEMI and IEEE. They contribute to defining equipment interoperability standards, process control protocols, and metrology guidelines that enhance manufacturing consistency and quality. LAM is involved in sustainability initiatives within the semiconductor industry in support of standards for environmental management, energy efficiency, and chemical safety. Their collaboration with federal agencies and industry consortia helps advance cybersecurity standards tailored to semiconductor fabrication environments, which helps reinforce supply chain security and resilience. Through these efforts, LAM Research supports ASCET's mission to promote robust, interoperable, and sustainable standards for CETs.

Micron Technology [64, 65, 66, 67]

Role in CET
Micron Technology specializes in memory and storage chips. In 2023, Micron recorded revenues of $15.54 billion in 2023, and Micron is one of three companies that collectively produce more than 90% of the world's DRAM chips. The company has offices globally and they products are typically used in automobiles, consumer electronics, servers, and computers.

Role in Standardization of CET
Micron Technology actively participates in semiconductor and microelectronics standardization through their membership in JEDEC and SEMI, including standards for memory interfaces, packaging, and manufacturing processes. Micron's involvement supports industry-wide alignment on quality and performance standards, particularly for DRAM and NOT AND (NAND) technologies.

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NVIDIA [68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78]

Role in CET

NVIDIA is a leading semiconductor and computing technology company. NVIDIA designs and develops integrated circuits, primarily graphics processing units (GPUs) and specialized chips used in computing, data centers, AI, and autonomous systems.

As a fabless company, NVIDIA manufactures most of their chips at Taiwan Semiconductor Manufacturing Company's (TSMC) Taiwan-based factories. TSMC is one of the few companies currently building plants in the United States. In 2025, they announced plans to build a third fab at TSMC Arizona and are expected to create 6,000 jobs and play a critical role in the onshoring of semiconductor manufacturing. In 2025, NVIDIA set a record by being the first company to reach $5 trillion in market valuation, indicating dominance not only in technology and semiconductors, but the broader U.S. economy.

Role in Standardization of CET

Beyond hardware innovation, NVIDIA has emerged as a key player in AI ethics and policy development, promoting responsible AI through fairness, bias mitigation, and transparency. The company supports tools enabling model interpretability such as gradient visualizations and debugging capabilities. NVIDIA collaborates with public and private organizations, including the U.S. Department of Energy (DOE), on ethical AI applications in climate modeling and drug discovery. They also contribute to industry benchmarks defining performance and fairness standards that help evaluate AI model robustness.

NVIDIA actively collaborates with ASCET-aligned standards groups and leading industry SDOs—such as IEEE, ISO/IEC, and various AI and semiconductor consortia—in areas including AI interoperability, GPU-accelerated computing, digital twin frameworks, and chiplet design standards. Through participation in workshops and consortia focused on next-generation microelectronics and CETs, NVIDIA supports broader industry alignment consistent with ASCET's objectives.

Qualcomm [79, 80, 81, 82, 83, 84]

Role in CET

Qualcomm is the world's largest fabless semiconductor company by chip design volume. They produce Systems on a Chip (SoCs) SoCs for smartphones, Internet of Things (IoT), automotive, networking, and AI-edge applications. Qualcomm drives innovation in 5G/6G, Wi-Fi, and AI-native capabilities. They are a significant player in powering global connectivity and emerging technology use cases.

Role in Standardization of CET

Qualcomm actively contributes to global standards development in wireless communications and semiconductor technologies. They play a key role in the 3rd Generation Partnership Project (3GPP) (covering 2G Code Division Multiple Access [CDMA] through 5G Advanced and early 6G pre-standardization), IEEE 802.11, Mobile Industry Processor Interface (MIPI), Wi-Fi Alliance, Bluetooth Special Interest Group (SIG), Open Radio Access Network (O-RAN) Alliance,

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Moving Picture Experts Group (MPEG), and others. While Qualcomm no longer chairs 3GPP Technical Specification Group (TSG) RAN, they remain a primary leader in key working groups such as RAN1. Qualcomm collaborates with ASCET-aligned standards groups and participates in workshops and consortia focused on next-generation microelectronics and CETs, supporting broader industry alignment consistent with ASCET's objectives.

Samsung Electronics [85, 86, 87, 88, 89]

Role in CET
Samsung Electronics is a global semiconductor leader with broad capabilities in memory (DRAM, NAND), logic chips, foundry services, and advanced packaging. They operate some of the world's most advanced fabrication facilities including a massive facility in South Korea (Pyeongtaek campus). Samsung drives innovation in next-generation process nodes (2nm and below), heterogeneous integration, and AI-optimized chips.

Role in Standardization of CET
Samsung actively participates in international and regional standards development organizations such as JEDEC, SEMI, IEEE, and ISO/IEC. They contribute to standards for memory interfaces, packaging, reliability testing, and advanced process technologies, and are actively involved in collaborative initiatives to develop standards for heterogeneous integration, chiplet interoperability, and energy-efficient semiconductor manufacturing. They also engage in sustainability efforts such as industry-wide frameworks for greenhouse gas emissions reduction and resource efficiency. Samsung's participation in standards bodies and consortia supports ASCET's mission through their focus on interoperability, quality, security, and sustainability in semiconductor technologies

Synopsys [90]

Role in CET
Synopsys is a leading provider of EDA solutions, Si IP, and system verification and validation. The company collaborates with semiconductor and systems companies to enhance their R&D capabilities. In 2025, Synopsys significantly expanded their capabilities in simulation and analysis through acquiring Ansys.

Role in Standardization of CET
Synopsys actively participates in IEEE standards committees.[91] Synopsys employees have engaged in international standards development with SDOs including IEEE, ISO, IEC, and SAE.[92]

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Texas Instruments (TI)[93, 94, 95, 96, 97]

Role in CET
Texas Instruments is a global semiconductor company that designs, manufactures, tests, and sells embedded and analog processing chips. This company is developing four 300-milimeter semiconductor wafer fabrication plants in Sherman, Texas. The complex is expected to manufacture more than 100 million chips daily and support up to 3,000 direct jobs.

Role in Standardization of CET
TI has been involved in automotive ISO/TS 16949 certification since 2004, which covers the design and manufacture of ICs for automotive applications. The company actively participates in industry standards development committees and associations such as IEEE and the Automotive Electronics Council (AEC); they are actively advancing semiconductor quality, reliability, and interoperability. TI aligns with ASCET's mission by contributing to standards that support critical and emerging technologies in semiconductors and microelectronics.

RELEVANT STANDARDS BODIES

This section identifies the primary SDOs involved in shaping the semiconductor standards environment. It highlights their roles, key initiatives, and contributions to semiconductor governance, ethics, performance, and interoperability. These organizations establish technical foundations for global supply chains by defining specifications for materials, devices, packaging, and testing. Their standards work focuses on reliability and interoperability, and they are actively addressing priorities in sustainability, cybersecurity, and advanced packaging for heterogeneous integration.

ASTM International

Role in Semi/Micro Standards
Global standards development for electronics and semiconductor materials: [98] Develops consensus-based standards that define testing methods, material specifications, and quality benchmarks for semiconductor fabrication and microelectronics; supports interoperability, reliability, and safety across global supply chains

Sets device and packaging reliability standards: [99] Provides test methods for wire bond strength, thermal stability of wafers, and metallization integrity; supports qualification of advanced packaging technologies like flip-chip and through-silicon vias (TSVs)

Sets standards for semiconductor-grade materials and contamination control:[100] Provides test methods for purity and contamination in gases, chemicals, and surfaces used in wafer fabrication; includes standards for oxygen, moisture, and hydrocarbon contribution from gas distribution components

Technical Committee (TC) F01 on Electronics:[101] Oversees standards development for semiconductor devices, bonding wires, contamination control,

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compound semiconductors, sputter metallization, and printed electronics; scope includes test methods, specifications, and guidance for materials and processes used in microelectronics manufacturing

Key Initiatives

Additive Manufacturing Center of Excellence (AM CoE):[102, 103, 104] Partners with industry to create certification pathways for AM in semiconductor equipment supply chains

Advancing Standardization for Critical and Emerging Technologies (ASCET) CoE:[105] Launched in partnership with NIST to accelerate U.S. leadership in international standards for CETs, including semiconductors and microelectronics; focuses on pre-standardization research, workforce development, and global engagement strategies

Enables supply chain traceability and security:[106, 107] Introduced a conformity assessment framework to enable supply chain traceability and verification using emerging technologies including blockchain, AI, and geospatial data; designed to strengthen compliance and transparency for critical materials and semiconductor-related supply chains

Environmental sustainability in semiconductor manufacturing:[108, 109] Aligns standards with global sustainability goals; focuses on reducing environmental impact in electronics and semiconductor supply chains; has initiatives that address lifecycle assessment, water efficiency, energy efficiency, and circularity in materials management for advanced manufacturing sectors

Metrology and measurement standards for semiconductor materials:[110, 111] ASTM Committee F01 develops standards for evaluating semiconductor substrates, thin films, and contamination control; includes guidance for testing resistivity and Hall coefficient in single-crystal semiconductors and contamination analysis for wafer fabrication environments

Automotive Electronics Council (AEC)

Role in Semi/Micro Standards

Defines global qualification requirements for automotive-grade semiconductors:[112] Maintains the widely adopted AEC-Q series standards (e.g., Q100 for ICs, Q101 for discrete semiconductors, Q102 for optoelectronics, Q200 for passive components); these standards ensure components can withstand extreme temperatures, mechanical stress, electrical loads, etc.

Focus on improving reliability and interoperability:[113] AEC standards aim to eliminate misunderstandings between manufacturers and purchasers, improve product quality, and facilitate interoperability for automotive electronics on a global scale

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Industry-led standard body for automotive electronics reliability:[114] AEC was established by Chrysler, Ford, and General Motors (GM) to create common qualification and quality-system standards for electronic components used in harsh automotive environments (high heat, vibration, long lifespan, etc.)

Key Initiatives

Copper wire interconnection qualification requirements (AEC-Q006):[115, 116] Specifies minimum reliability testing requirements for semiconductor devices that use copper wire bonding instead of traditional gold; ensures robust performance of copper-based interconnects under automotive stress conditions including thermal cycling and mechanical integrity; mandatory prerequisite for achieving compliance with ISO 26262 (i.e., international standard for functional safety of electrical and electronic systems in road vehicles)

Discrete semiconductor durability standards (AEC-Q101):[117] Defines qualification requirements for automotive systems including diodes, transistors, and metal-oxide-semiconductor field-effect transistors (MOSFETS); focuses on performance under thermal cycling, electrical overstress, and humidity exposure to ensure operation in safety-critical environments

Integrated circuit reliability qualification (AEC-Q100):[118] Establishes stress-test protocols for automotive grade ICs to test their reliability under extreme conditions (e.g., thermal, electrical, mechanical), electrostatic discharge (human body model / charge device model [CDM]), latch-up, early life failure rate (ELFR), and high-temperature operating life for mission-critical semiconductor devices

- **Advanced semiconductor reliability enhancements (AEC-Q100 Revision J):**[119] Expands guidance for smaller process nodes (≤14nm), thermal/power cycling, and failure analysis to address challenges in EV power electronics and high-performance computing (HPC) for autonomous vehicles

Multi-chip module reliability guidelines (AEC-Q104):[120] Sets qualification criteria for complex semiconductor assemblies integrating multiple chiplets; addresses package integrity, interconnect reliability, thermal management, electrostatic discharge, solder joint durability, mechanical integrity, and other areas for next-generation automotive electronics

Optoelectronic component qualification framework (AEC-Q102):[121] Reliability standards for optoelectronic components/devices (e.g., LEDs) in automotive lighting/sensing applications; addresses vibration resistance, thermal shock, electrical performance, environmental exposure, and mechanical integrity for advanced driver-assist systems (ADAS)

Passive component stress-test protocols (AEC-Q200):[122] Sets qualification methods for resistors, capacitors, inductors, and other related components to

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withstand high vibration, extreme temperatures, and electrical load variations; ensures consistent performance in power electronics including infotainment systems

CEN-CENELEC

Role in Semi/Micro Standards

Coordination with international standards:[123, 124, 125] CEN-CENELEC aligns European and global standards through cooperation with ISO and IEC; new standards projects are jointly planned between CEN-CENELEC, ISO, and IEC to avoid duplicate work and ensure European needs are met by international standards

Pan-European consensus standards body:[126, 127, 128] CEN and CENELEC are among three officially recognized European SDOs (alongside ETSI) under EU and European Free Trade Association (EFTA) mandates; they develop standards through an established consensus process among national standards bodies in 34 countries [129, 130]

Key Initiatives

Chip security & certification standards:[131, 132, 133] CEN-CENELEC established a "semiconductor devices and trusted chips" technical committee (i.e., CLC/TC 47X) in response to Europe's 2022 Standardization Strategy, which highlighted the urgent need for "common standards for trusted and secure chips;" CLC/TC 47X develops EU-wide standards for chip cybersecurity and reliability and is actively developing a semiconductor security standards roadmap for Europe's semiconductor supply chain

European Chips Act standardization roadmap:[134] Through its support of the EU Chips Act (2023), CEN-CENELEC and the European Commission initiated a push to identify standards gaps and coordinate the development of critical semiconductors standards; CEN-CENELC co-hosted a "Trusted Chips" workshop in 2022 to map out needs in chip security and supply chain trust, which led to the development of a joint semiconductor standardization roadmap for Europe

Transatlantic standards alignment efforts:[135, 136] CEN participates in EU-U.S. cooperation on semiconductor standards; CEN works alongside other European stakeholders through venues like the EU-U.S. Trade & Technology Council (TTC) and coordinates with U.S. counterparts to avoid divergent standards and promote international, industry-led standards as the foundation for chip technologies

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Electrostatic Discharge Association (EOS/ESDA)

Role in Semi/Micro Standards

ANSI-accredited standards developer for electrostatic control:[137, 138, 139] As of 2025, EOS/ESDA is the only ANSI-accredited organization that writes and publishes standards on electrostatics and electrostatic control; their work includes development of 70+ standards, test methods, and technical reports addressing electrostatic discharge (ESD) and electrical overstress (EOS) in electronics manufacturing environments, semiconductor fabs, assembly lines, testing environments, repair environments, and others; EOS/ESDA standards define best practices for ESD control programs, device qualification, and compliance verification to protect sensitive microelectronic components from damage during design, handling, and packaging

Provides global benchmark for integrating ESD control programs:[140, 141] Developed a joint standard with ANSI—ANSI/ESD/S20.20—which serves as the global benchmark for developing and implementing ESD control programs in semiconductor and electronics manufacturing; outlines administrative and technical requirements for grounding, protected areas, packaging, and compliance verification to minimize ESD-related failures in ICs, printed circuit boards (PCBs), and advanced packaging technologies

Key Initiatives

Compliance verification and auditing tools:[142, 143] EOS/ESDA promotes American National Standards Institute (ANSI)/ESD S20.20 compliance through structured auditing programs and advanced tools like EOS/ESD Audit Kits, which allow for verification of surface resistance, grounding integrity and grounding system performance, ionization system performance, and detection of harmful ESD/EOS events

Facility and personal certification programs:[144, 145] EOS/ESDA offers an ANSI-based facility certification (i.e., ANSI/ESD S20.20) including professional credentials[146] for ensuring compliance and expertise in ESD control; the EOS/ESDA certification programs help semiconductor fabs and electronics manufacturers reduce ESD-related yield loss and improve reliability

Global standards collaboration and education:[147, 148] EOS/ESDA partners with adjacent organizations (i.e., IEC TC101 and JEDEC) on harmonized standards; EOS/ESDA also holds an annual EOS/ESD Symposium and online training programs for semiconductor professionals that cover device-level ESD design, system-level protection, test methods, packaging principles, compliance auditing, and others

Technology roadmap for ESD control: [149, 150] EOS/ESDA publishes an annual technology roadmap that projects future ESD sensitivity thresholds for semiconductor devices and their impact on ESD control practices; long-term focus of the roadmap is through 2030; roadmap addresses trends in device testing, latch-

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up design, and advanced packaging challenges including for 2.5D/3D ICs and multi-chip modules

European Telecommunications Standards Institute (ETSI)

Role in Semi/Micro Standards

Global alignment of connectivity standards: [151, 152] ETSI participates in the 3rd Generation Partnership Project (3GPP), which globally comprises SDOs responsible for developing cellular mobile system specs; ETSI contributes to internationally harmonized standards for mobile communications and contributes to globally applicable specs for machine-to-machine and IoT communications

Pan-European consensus standards:[153, 154] ETSI is one of three predominant European Standards Organizations (with CEN and CENELEC); serves as Europe's primary SDO for telecommunications, broadcasting, and other electronic communications networks and services; and operates an open, direct-membership model with more than 900 organizations from more than 60 countries

Key Initiatives

Developed baseline cybersecurity requirements standard for consumer IoT devices:[155, 156] ETSI published EN 303 645, which sets baseline cybersecurity requirements for consumer IoT devices; the standard promotes security-by-design and provides high-level provisions and implementation guidance relevant to connected products and the broader device ecosystems in which semiconductor components are embedded

Leader in mobile communications standardization:[157, 158, 159] ETSI contributes to European and global mobile standards including Global System for Mobile Communications (GSM), 4G, and 5G systems; ETSI helps coordinate European stakeholder contributions to consensus-based specifications for mobile systems; ETSI maintains an active role with 3GPP in contributing to future 6G specifications

Open network architectures and edge computing:[160, 161] ETSI has developed influential work on Network Functions Virtualization (NFV) and Multi-access Edge Computing (MEC), which define open, interoperable, cloud- and edge-oriented telecom architectures; ETSI's work on NFV and MEC is relevant to semiconductor and microelectronics applications because it shapes technical requirements for communications and edge-computing environments in which advanced hardware is deployed

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Institute of Electrical and Electronics Engineers (IEEE) Standards Association (SA)

Role in Semi/Micro Standards

Global standards development for electronics, computing, and semiconductor technologies:[162] One of the world's largest technical professional organizations; leading developer of international standards for interoperability, safety, and performance across electronics and computing systems; developed standards for design verification, testing, and security requirements of ICs, microelectronics, advanced packaging, etc.; IEEE develops standards that support design automation, low-power ICs, advanced test architectures, supply chain security, digital manufacturing, etc.:

- **IEEE 1149.x:**[163] Boundary-scan and test access architectures
- **IEEE 1801:**[164] Low-power IC design and verification

Industry collaboration for semiconductor and microelectronics standardization:[165] Actively participates in strategic initiatives like the CHIPS R&D Standards Program; collaborates with organizations like ANSI, IPC, and SEMI to accelerate standards development for advanced packaging, heterogeneous integration, and chiplet-based architectures; their efforts, specifically with CHIPS, aim to align standards with rapid innovation cycles in semiconductor manufacturing[166]

Key Initiatives

Boundary-scan and test access architecture standards (IEEE 1149.X series):[167, 168] Establishes protocols for testing interconnections within ICs and complex systems; purpose is to enable efficient fault detection and improve reliability in advanced packaging and 3D ICs

Heterogeneous Integration Roadmap (HIR):[169] HIR was sponsored by IEEE Electronics Packaging Society (EPS), SEMI, and other partners, to provide pre-competitive pathways for integrating multiple semiconductor technologies (logic, memory, photonics, radio frequency [RF]) into advanced packages; addresses technical challenges in 2.5D/3D integration, chiplet architectures, thermal management, and system co-design

IEEE Circuits and Systems Society Standards Activities (CASS SASAD):[170, 171] The Standards Activities Subdivision (SASD) was established to develop standards for emerging semiconductor technologies, such as:

- **Design and Test for Emerging Circuits and Systems (ICSC)**
- **Domain-Specific Accelerators (DSASC):** Standards for design, evaluation, and testing of accelerators for AI, encryption, and multimedia processing
- **Flexible and Wearable Circuits and Systems (FWSC):** Standards for design and testing of flexible electronics, e-textiles, wearable devices
- **Hardware Security Standards Committee (HSSC):** Standards addressing hardware-level security vulnerabilities and mitigation strategies for semiconductor devices

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IEEE Industry Connections Program:[172] Program incubates new standards and collaborative projects for rapidly evolving technologies including semiconductor design, packaging, and security; the program provides a platform for industry, academia, and government to co-develop guidelines, white papers, technical reports, position papers, case studies, roadmaps, proposals for standards, and pre-standardization frameworks

IEEE International Roadmap for Devices and Systems (IRDS):[173, 174] IRDS is a global strategic roadmap that guides the future of microelectronics, spanning devices, systems, and integration technologies; the roadmap provides long-term forecasts and identifies critical challenges for advanced semiconductor design, manufacturing, and packaging; IRDS has been adopted as a reference by major programs such as the European Chips Act, Japan's semiconductor strategy, and U.S. CHIPS Act initiatives

Low-power IC design and verification (IEEE 1801):[175] Defines methods for specifying and verifying power intent in IC designs in support of energy-efficient architectures for mobile and high-performance systems

Wearable consumer electronics architecture (IEEE 360):[176, 177] Gives an overview and technical requirements for wearable devices; focuses on reliability, safety, and interoperability guidelines for health, fitness, and infotainment applications

International Electrotechnical Commission (IEC)

Role in Semi/Micro Standards

Global standards development for electronic components:[178] IEC develops international standards that define safety, reliability, and performance requirements for electronic/electrical technology; IEC standards cover discrete devices, ICs, Micro-Electro-Mechanical Systems (MEMS), fiber optics, and printed electronics; IEC standards provide test methods, qualification protocols, and performance benchmarks for enabling interoperability and enhancing product quality[179]

Technical leadership through committees on device-level and system-level standards:[180, 181] IEC organizes its work through TCs on semiconductor devices (TC 47), fiber optics (TC 86), and printed electronics (TC 119); defines test methods, performance benchmarks, qualification protocols, etc., for components and assemblies; and specifications for electrical, mechanical, and environmental performance; IEC's mission is focused on ensuring products meet international requirements for reliability and safety[182]

Key Initiatives

IEC TC 47 Semiconductor devices:[183] Develops standards for semiconductor devices and ICs; subcommittees address ICs (SC 47A), packaging (SC 47D), discrete devices (SC 47E), and MEMS (SC 47F);

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Key standards include:
- **IEC 60749 series:**[184] Mechanical and climatic test methods
- **IEC 63287-1:**[185] Reliability qualification guidelines for ICs
- **IEC TC 86 Fiber Optics:** Prepares standards for fiber optic systems, modules, devices, and components used in communications equipment; scope includes terminology, optical and mechanical requirements, calibration and measurement methods, environmental testing, etc.
- **IEC 61280 and IEC 61300:**[186, 187] Defines test procedures for optical performance and reliability

IEC TC 119 Printed Electronics:[188] Prepares standards for printed electronics; covers terminology, materials (conductive inks, substrates, etc.), processes, equipment, and quality assessment

IEC 62899 series:[189] Test methods for conductive ink, substrate properties; printability requirements for flexible and wearable electronics

International Organization for Standardization (ISO)

Role in Semi/Micro Standards

Contamination control and cleanroom standards: ISO provides critical manufacturing process standards for semiconductors; ISO 14664 serves as the global benchmark for cleanroom air cleanliness and is a key factor for yield and device reliability in wafer fabrication[190]

Functional safety in automotive semiconductors: ISO develops standards for safety-critical chip design such as ISO 26262, which provides guidelines to ensure advanced automotive chips (for ADAS, EV control, etc.) achieve near-zero failure rates over a vehicle's lifespan[191]

Global consensus standards for microelectronics and semiconductors: ISO publishes internationally agreed standards that ensure reliability, quality, and interoperability in products and products worldwide; ISO's global frameworks provide common technical foundations that enable cross-border collaboration and supply chain cohesion in the semiconductor industry [192]

Quality management and supply chain reliability: Major semiconductor manufacturers adopt ISO's standards to drive consistent product quality and traceability; ISO 9001 is a foundational certification held by fabricators worldwide since the 1990s; International Automotive Task Force (IATF) 16949:2016 is an automotive-specific quality framework based on ISO 9001 that chipmakers use for meeting safety and reliability requirements for vehicle-grade semiconductors[193, 194,

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Key Initiatives

Collaboration on emerging technology standards: Through ISO/IEC JTC 1, ISO co-develops cutting-edge IT standards for semiconductors; JTC 1's subcommittees (e.g., on AI and IoT) produce globally unified specifications that incorporate software and hardware considerations [195]

- **Supply chain security and resilience:** ISO introduced standards ,[200] to improve supply chain security [196, 197]
- **ISO 28000:2022 for supply chain security management systems:** ISO 28000:2022 is a globally recognized framework that helps with vulnerability identification for protecting the flow of semiconductor materials and products against threats like counterfeit components, logistic disruptions, and physical tampering
- **ISO/IEC 27001 for information security management:** ISO/IEC 27001 helps safeguard sensitive design data and intellectual property to ensure trustworthy operations across global R&D and manufacturing networks

Sustainability and environmental standards: ISO drives sustainable practices in semiconductor manufacturing through globally adopted frameworks like ISO 14001 and ISO 50001 [198, 199, 200]

- **ISO 14001 for environmental management systems:** ISO 14001 is used worldwide by chip fabricators, including all TI and NXP manufacturing sites, for reducing environmental impact, managing emissions, and ensuring regulatory compliance
- **ISO 50001 for energy management:** ISO 50001 is used for energy use optimization, resource efficiency, and emissions reduction

IPC International, Inc.

Role in Semi/Micro Standards

Accredited ANSI standards developer with global reach: [201, 202, 203] Accredited by ANSI; recognized internationally; publishes widely used documents that serve as benchmarks for workmanship and reliability in electronic assemblies

- **IPC-A-610:**[204] Standards for acceptability of electronic assemblies
- **IPC-J-STD-001:**[205, 206, 207] Requirements for soldered electrical and electronic assemblies

Expanding scope to advanced packaging and semiconductor ecosystem:[208, 209] IPC broadened their standards development beyond PCBs to include IC substrates, system-in-package technologies, and sustainability initiatives; they collaborate with industry and government on advanced packaging strategies[210] to strengthen semiconductor supply chains and support emerging technologies

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Global standards developer for electronics manufacturing and assembly:[211, 212, 213] Leading standard organization focused on PCBs, electronic assemblies, electronics repair, digital data exchange, packaging technologies, etc.; their standards define best practices for design, fabrication, assembly, and inspection of electronic products; IPC standards center around quality, reliability, and consistency, and are widely adopted across aerospace, automotive, medical devices, and advanced microelectronics sectors

Key Initiatives

Acceptability and workmanship standards for electronic assemblies (IPC-A-610):[214, 215] Represents the most widely used standard for defining visual acceptance criteria for soldered electronic assemblies; classifies products into three categories based on reliability requirements: consumer, industrial, and high-reliability applications); provides guidance for solder joints, component placement, coatings and protection, identification and repair, cleanliness, and others

Advanced packaging and microelectronics roadmap participation (MAPT Roadmap):[216, 217] Collaborated with Semiconductor Research Corporation (SRC) and other stakeholders on the *Microelectronics and Advanced Packaging Technologies (MAPT) Roadmap,* which addresses next-gen packaging, heterogeneous integration, and supply chain strategies to support CHIPS Act objectives and U.S. semiconductor leadership

Cybersecurity and digital manufacturing standards (IPC-1792 and IPC-2591 CFX):[218, 219, 220] IPC-1792 provides guidelines for cybersecurity risk mitigation in electronics manufacturing; IPC-2591 enables machine-to-machine communication for smart factories that support Industry 4.0 adoption

Requirements for soldered electrical and electronic assemblies (IPC-J-STD-001):[221] Establishes materials, methods, and validation criteria for producing high-quality soldered interconnections; used for ensuring reliability in harsh environments such as aerospace and defense

JEDEC Solid State Technology Association

Role in Semi/Micro Standards

Global standard development for microelectronics:[222, 223] Serves as a leading international standards organization; creates open, consensus-based standards for semiconductors, memory devices, microelectronics packaging, power management, thermal management, solid-state storage, interfaces, chiplets, and several other topic areas; JEDEC standards focus on interoperability, reliability, and performance consistency across the global electronics supply chain; JEDEC standards are made freely available and are widely adopted by manufacturers

Key Initiatives

Chiplet interoperability and digital model framework (JEP30 + OCP CDXML):[224, 225, 226] Standardizes digital descriptions for chiplets to enable automated

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System in Package (SiP) design and cross-vendor compatibility; supports modular semiconductor integration and accelerates heterogeneous packaging innovation

Enhanced NAND flash interface protocol (JESD230G):[227, 228, 229, 230] Defines signaling and command/address protocols for NAND-based storage devices; supports high data transfer rates of up to 4.8 GT/s; introduces the "Separate Command/Address (SCA)" protocol to improve throughput and reduce latency in solid-state storage systems

High-bandwidth 3D memory architecture (HBM4, JESD270-4):[231, 232, 233] Establishes specs for stacked memory modules that deliver ultra-high throughput for GPUs, AI accelerators, and HPC systems; HBM4 doubles bandwidth compared to HBM3 and adds more channels and improves power efficiency for performance-critical environments

Next-generation DRAM interface standards (DDR5 and LPDDR6):[234, 235, 236] Defines electrical and protocol-level requirements for high-speed DRAM used in PCs, servers, and mobile devices; DDR5 improves bandwidth and efficiency for data-intensive workloads; LPDDR6 achieves high data transfer rates through advanced power-saving features

Thermal characterization and reliability qualification standards (JESD51 and JESD22 series):[237, 238] Provides methods for measuring thermal resistance and managing heat dissipation in IC packages; includes stress-test protocols for reliability under temperature cycling, humidity bias, mechanical shock, etc.

SAE International

Role in Semi/Micro Standards

Automotive and mobility standards development with semiconductor relevance:[239, 240] Develops standards for automotive and mobility applications through technical committees focused on vehicle electrical and electronic systems; cybersecurity, and functional safety; SAE International's work is relevant to automotive electronics supply chains and systems that incorporate semiconductor components; SAE's standards are primarily framed at the vehicle system level rather than as semiconductor-specific standards

Key Initiatives

Automotive functional safety guidance aligned with key ISO standard (ISO 26262):[241, 242] SAE's Functional Safety Committee publishes work such as J2980_202310, which presents a method for Automotive Safety Integrity Level (ASIL) determination for automotive motion-control electrical and electronic systems and is intended to be consistent with ISO 26262 (i.e., the international standard for functional safety of road-vehicle electrical and electronic systems); SAE's role is grounded in automotive functional-safety engineering and does not explicitly provide semiconductor-specific guidance

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Cybersecurity guidance for cyber-physical vehicle systems:[243] SAE International published J3061, which provides lifecycle cybersecurity guidance for cyber-physical vehicle systems including computer software and hardware components; the guidebook establishes foundational cybersecurity principles for the automotive vehicle industry

Joint automotive cybersecurity standard development:[244] SAE co-developed ISO/SAE 21434:2021, which defines cybersecurity engineering requirements for road-vehicle electrical and electronic systems, including components and interfaces; ISO/SAE 21434:2021 is relevant to automotive systems and supply chains that include semiconductor components

Semiconductor device robustness validation for automotive applications:[245, 246] SAE maintains J1879_201402 (Handbook for Robustness Validation of Semiconductor Devices in Automotive Applications), which explicitly states that semiconductor device qualification is the main scope of the document and focuses primarily on integrated circuit subjects for automotive electronics

Semiconductor Equipment and Materials International (SEMI)

Role in Semi/Micro Standards
Policy Advocacy: SEMI has government relations programs in the United States, Europe, and Asia dedicated to raising awareness around the semiconductor equipment and materials industry

Standards Development: SEMI is the leading microelectronics industry association and provides the foundation for electronics manufacturing innovation. SEMI Standards cover 3D-IC, equipment automation (hardware and software), flat-panel displays, facilities, gases, high brightness LED, MEMS / Nanoelectromechanical Systems (NEMS), materials, microlithography, packaging, photovoltaic, process chemicals, silicon material and process control, and traceability. Guidelines are also developed to cover safety-related issues.[247] The SEMI International Standards Program is a key service offered by SEMI for the benefit of the worldwide electronics design and manufacturing industries

Key Initiatives
CHIPS Act Workforce Development: SEMI plays a critical role in supporting the implementation of the CHIPS act. The SEMI foundation offers guidance to companies submitting applications for CHIPS funding. SEMI is recognized as a strategic partner by the NIST in the CHIPS Workforce Development Guide[248]

Global SEMI Standards Summit: SEMI held its first-ever Global Standards Summit, SEMICON, in Japan in 2024. The event covered several critical topics such as advanced packaging architectures and materials, cybersecurity, and supply chain [249]

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National Network of Microelectronics Education (NNME): A national program that aims to build centers around the United States for microelectronics education and training[250]

Semiconductor Climate Consortium (SCC): Established under SEMI, SCC focuses on decarbonization and transparency in semiconductor manufacturing[251]

EXISTING STANDARDS

The table below provides a curated selection of existing standards in semiconductors and microelectronics, grouped into broad categories. This list is not exhaustive; instead, it highlights representative standards and areas of relevance to this scan's focus. Inclusion is guided by criteria such as relevance to critical technology segments, prominence industry practice, and impact on U.S. semiconductor leadership. The intent is to orient readers to key parts of the standards landscape (e.g., manufacturing processes, device reliability, application-specific requirements) without cataloging every standard in the field.

Automotive semiconductor reliability and safety
- AEC Q100
- ISO 26262-11[252, 253]

Description
Encompasses standards ensuring that automotive semiconductor components meet stringent reliability and safety requirements. ISO 26262-11 offers guidelines to integrate semiconductor devices into the automotive functional safety lifecycle (defining chip-level ASIL development and verification practices); AEC-Q100 mandates rigorous stress-test qualification of automotive-grade integrated circuits to ensure robust performance and reliability under harsh conditions

Chemical purity and equipment safety
- SEMI C1, C10, S2 [254, 255, 256, 257, 258, 259, 260]

Description
SEMI C-series standards specify purity levels and testing methods for chemicals used in semiconductor manufacturing; SEMI S2 provides safety guidelines for manufacturing equipment to protect workers and maintain cleanroom integrity

Computer numerical control (CNC) process data for additive manufacturing (AM)
- ISO 14649-17 (STEP-NC)[261, 262, 263, 264]

Description
Defines a standardized data model for CNC machines to communicate process plans for AM, enabling consistent and interoperable production workflows across different equipment

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Memory module specifications
– JEDEC JESD79 (DDR), JESD271 (HBM4) [265, 266, 267, 268, 269, 270]

Description
Sets the standards for dynamic random-access memory (DRAM) modules like DDR and high-bandwidth memory (HBM4); covers electrical, mechanical, and thermal requirements to ensure interoperability and reliable performance across manufacturers

Printed circuit board (PCB) and assembly quality
– IPC A-610, A-600, J-STD-001, IPC-7711/21 [271, 272, 273, 274, 275, 276, 277, 278, 279, 280, 281]

Description
Provides guidelines for acceptable quality levels in PCB fabrication and assembly, including soldering processes, inspection criteria, rework procedures, and cable/harness assembly standards to ensure product reliability and manufacturability

Semiconductor device design and testing
– IEC 60747 series [282, 283, 284]

Description
Covers standards for discrete semiconductor devices and ICs, including specifications for device performance, reliability, testing methods, and packaging to ensure consistent quality and functionality

Silicon (Si) wafer dimensions and quality
– SEMI M1 [285, 286, 287, 288]

Description
SEMI M1 defines the critical physical dimensions and quality characteristics for polished single-crystal Si wafers used in semiconductor manufacturing, including diameter, thickness, flatness, and edge features to ensure compatibility with processing equipment

RELEVANT ROADMAPS AND STRATEGY DOCUMENTS

This subsection provides an overview of influential roadmaps, strategic plans, and policy frameworks shaping standards for semiconductors and microelectronics. These documents outline long-term technology trajectories, identify critical gaps, and set priorities for coordinated action across industry, government, and research communities. Collectively, they address areas such as advanced packaging, heterogeneous integration, sustainability, security, and workforce development; they offer insights into how global strategies are driving standards alignment for next-generation semiconductor ecosystems.

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EOS/ESDA Electrostatic Discharge Technology Roadmap [289]

EOS/ESD Association, 2025

Focus

The roadmap outlines how ongoing advances in semiconductors and microelectronics (e.g., smaller geometries, faster input/output [I/O] speeds, new packaging architectures) are making devices more vulnerable to static-related damage. The roadmap notes that as vulnerabilities increase, there will be a need for updated ESD standards including modernized test methods, revised qualification expectations, stronger manufacturing control requirements, clearer guidance for complex package types, and improved approaches to evaluating system-level behavior. Existing standards must evolve to reflect new packaging architectures, faster interfaces, and increasingly delicate materials so that reliability can be maintained throughout design, qualification, production, and integration.

Goals

- Ensure system-level ESD practices evolve beyond legacy assumptions tied to component-level ratings
- Prepare standards bodies for new device categories (advanced packaging, photonics, next-generation power devices) that behave differently under ESD stress
- Provide a unified view of expected declines in device ESD tolerance to help guide updates to industry standards
- Strengthen standards for device-level testing, qualification, and process controls as technologies scale

Challenges/Barriers:

- Advanced packaging (e.g., chiplets, 2.5D/3D structures) introduces internal connections that current standards do not fully address
- High-performance devices face tradeoffs between meeting ESD expectations and maintaining electrical performance
- Manufacturing processes require tighter controls as device sensitivity continues to decline
- Smaller geometries and high-speed interfaces leave less room for protection, reducing allowable ESD levels
- System-level ESD failures often differ from device-level behavior, exposing gaps in today's standards

Opportunities/Recommendations:

- Develop new standards focused on technologies such as GaN, photonics, and highly scaled complementary metal–oxide–semiconductor (CMOS)
- Expand system-level standards to better capture real-world interactions across products, connectors, and assemblies
- Integrate simulation, modeling, and data-driven tools into ESD design and verification best practices
- Modernize component-level ESD test standards to reflect lower thresholds and new packaging designs
- Strengthen manufacturing standards by clarifying expectations for monitoring, grounding, and process capability

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Federal Semiconductors & Microelectronics Standards Working Group (SMSWG) Annual Report/ Priorities [290]

NIST, 2024

Focus
The report focuses on coordinating federal agency efforts in semiconductor and microelectronics standards development. It calls for voluntary consensus standards led by the private sector with federal support and aligns with the U.S. Government National Standards Strategy for Critical and Emerging Technology (NSSCET). The document addresses the entire semiconductor lifecycle, including design, manufacturing, packaging, testing, and supply chain security.

Key Strategy Areas
- **Chiplets:** Promoting modular semiconductor designs through chiplets with advanced packaging, interoperability, and interconnect standards to improve scalability and cost efficiency
- **Digital Twin:** Leveraging virtual replicas of manufacturing processes and supply chains to optimize production, quality control, and predictive maintenance
- **Metrology and Measurement Science:** Developing precise measurement techniques and standards critical for advanced packaging, manufacturing process control, and material integrity
- **Supply Chain and Security:** Ensuring integrity, authenticity, and availability of semiconductor components across global supply chains, addressing counterfeit detection, secure processors, and holistic security frameworks

Challenges
- Fragmented standards landscape with no unified body overseeing secure processors
- Insufficient integration of cyber assurance and anti-tamper measures
- Lack of standardized test articles and verification methods for counterfeit detection
- Limited standards for digital twin interoperability and lifecycle management
- Need for advanced thermal management and power delivery standards in chiplet packaging

Recommendations
Advance metrology standards for thermal management and defect inspection

- Develop open standards for chiplet packaging and interconnects (e.g., Universal Chiplet Interconnect Express [UCIe])
- Establish unified frameworks for secure processors and supply chain transparency
- Promote comprehensive digital twin standards to enhance manufacturing efficiency
- Support emerging technologies like AI accelerator chips and photonics integration

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iNEMI Board Assembly Technology Roadmap [291]

International Electronics Manufacturing Initiative (iNEMI), 2025

Focus

iNEMI's roadmap examines how increasing miniaturization, densification, and the mix of very small and very large components on printed circuit boards are reshaping board assembly practices. It addresses the need for updated processes, materials, and manufacturing controls to maintain reliability as spacing shrinks, thermal demands increase, materials face new regulatory pressures, and system-level design choices directly impact manufacturability and rework. The roadmap also calls for expanding sustainability considerations, greater automation, and the need for stronger design-for-assembly and design-for-rework guidance across the electronics manufacturing ecosystem.

Goals

- Advance automation and process control to improve consistency, reduce manual intervention, and meet throughput demands
- Encourage design practices that anticipate manufacturability, test access, rework feasibility, and thermal behavior
- Improve process capability across printing, reflow, placement, soldering, and rework to support increasingly dense, mixed-component boards
- Strengthen industry alignment on assembly materials requirements, including low-voiding, low-temperature, and high-reliability formulations under evolving regulatory constraints
- Challenges/Barriers:
- Cleaning, no-clean residues, and conformal-coating interactions raise reliability concerns as materials interact with shrinking geometries
- Larger components introduce warpage, thermal mass, and co-planarity issues that complicate mixed-technology assemblies
- Limited test-point access on dense boards challenges functional and in-circuit testing strategies
- Miniaturization and tighter spacing constrain material performance, printing precision, and rework feasibility
- Press-fit and socket technologies face increased signal-integrity, current-carrying, and mechanical-loading requirements as system bandwidth and CPU demands rise
- Rework can unintentionally impact nearby components due to local heating, insufficient data from component suppliers, or inadequate design-for-rework considerations

Opportunities/Recommendations

- Advance printing technologies (e.g., high-accuracy stencils, laser-cut improvements, automated inspection) to support small apertures and mixed assemblies
- Develop improved assembly materials (e.g., finer solder paste types, low-voiding thermal interface materials [TIMs], more robust fluxes) matched to miniaturized and high-density layouts
- Enhance automation across placement, soldering, inspection, and rework processes to improve yield and reduce operator-dependent variability

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- Evolve press-fit and CPU socket designs using improved materials, optimized geometries, and better warpage control to meet next-generation system demands
- Integrate manufacturability, rework, and test needs earlier in board and component design to reduce downstream failures
- Modernize reflow oven design for energy efficiency, reduced nitrogen use, better flux extraction, and tighter thermal control across mixed-component assemblies

International Roadmap for Devices and Systems (IRDS), 2024 Edition

IEEE, 2024

Focus
IRDS provides a cross-industry, future-looking roadmap that identifies the technical, environmental, and manufacturing challenges that require new or updated semiconductor standards to enable next-generation semiconductor technologies and ensure that fabs remain reliable, scalable, compliant, and environmentally sustainable.

Key roadmap documents analyzed include
- Environmental Sustainability of Semiconductor Facilities (ESSF)[292]
- Lithography & Patterning [293]
- Outside System Connectivity (OSC) [294]

Challenges/Barriers – ESSF
- Brine management remains energy-intensive, costly, and technologically immature
- Cooling tower evaporation remains the single largest water loss in fabs
- Facility metering and monitoring systems are fragmented and poorly integrated for decision-making
- PFAS detection and removal methods are insufficient for extremely low concentration requirements
- Tool water consumption includes significant non-beneficial use, such as idle rinses and constant flows
- Water recycling back to ultrapure water (UPW) quality is limited by contaminants, dissolved solids, and mixed drain streams

Opportunities/Recommendations – ESSF
- Circular chemical recovery approaches for acids, solvents, and fluorinated byproducts
- Digital twins for real-time water and energy optimization using IRDS water and energy models
- Heat recovery and electrification of facility systems to lower energy and emissions
- Modernized drain segregation designs enabling higher water recycling and reduced cross-contamination
- Updates to SEMI S23, F98, F61, and F63 to incorporate new key performance indicators (KPIs) for water, energy, and chemical use

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Challenges/Barriers – OSC
- Data center networks increasingly limited by electrical interconnect reach and rising power consumption
- Fragmented IoT / Internet of Everything (IoE) connectivity protocols with inconsistent security models
- High cost, packaging complexity, and thermal constraints hinder widespread optical interconnect deployment
- Lack of unified interoperability standards for chiplet-level optical and electrical I/O
- RF front-end inefficiency at high frequencies due to high Analog-to-Digital Converter (ADC) / Digital-to-Analog Converter (DAC) power and low power-added efficiency (PAE)

Opportunities – OSC
- Advanced packaging approaches to integrate RF components, antennas, and photonics
- AI / machine learning (ML)-based optimization of spectrum, routing, and power management across network layers
- All-optical switching and routing to reduce latency and energy associated with optical-electrical conversions
- Emerging quantum photonic and cryogenic interconnect technologies for future systems
- Si photonics for high-bandwidth, low-latency chiplet and data-center interconnects

Challenges/Barriers – Lithography & Patterning:
- Backside patterning requires new alignment, etch, and cleaning capabilities not yet fully established
- High Numerical Aperture (NA) extreme ultraviolet (EUV) exposure field halving requires stitching or tiling solutions that are not yet mature
- Line-edge roughness becomes more severe with thinning resists and smaller features
- Mask manufacturing, inspection, and repair struggle with curvilinear designs and new absorber materials
- Resist materials face challenges including the need for per- and polyfluoroalkyl substance (PFAS)-free alternatives and tradeoffs with metal-oxide resists
- Stochastic defectivity limits EUV and High-NA scaling due to photon shot noise and resist chemistry randomness

Opportunities – Lithography & Patterning:
- AI/ML-driven prediction and mitigation of stochastic defects and overlay errors
- Backside metal patterning to improve power delivery and support next-generation logic scaling
- Directed self-assembly for pattern rectification and reduced stochastic defectivity

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- High-NA EUV enabling finer resolution and extending optical lithography scaling
- Hybrid X-ray and e-beam metrology for buried feature and 3D structure characterization
- Nanoimprint lithography for periodic memory layers and specialized patterning steps
- Sustainability improvements including hydrogen recycling and reduced multi-patterning steps through EUV

SEMI Advanced Packaging & Heterogeneous Integration Roadmap (HIR) [295]

IEEE, 2024

Focus
This roadmap serves as a practical guide for the global electronics industry. It outlines the expected technology needs and areas where innovation is likely to advance over the next 15 years. The roadmap was developed collaboratively by IEEE (EPS, EDS, Photonics), SEMI, and American Society of Mechanical Engineers (ASME); it establishes a long-term, pre-competitive vision for progress in heterogeneous integration and advanced packaging.

The 2024 edition is available only as individual chapters rather than a single consolidated document:

HIR Chapter 17 Test Technology: Electrical & functional testing — Highlights the growing need for consistent testing methods and measurement standards so that increasingly complex chips can be validated reliably across companies and manufacturing lines

HIR Chapter 21 SiP and Module: Package-level design rules & qualification — Emphasizes the need for shared design rules, data formats, and manufacturing practices that allow different companies' components to be combined into compact modules without compatibility or reliability issues

HIR Chapter 22 Interconnects (2D/3D): Chiplet & die-to-die interfaces, interconnect standards — Calls for a common, industry-wide vocabulary and a set of agreed-upon metrics for describing how chips connect to one another to enable consistent comparison and interoperability across future packaging approaches

HIR Chapter 23 Wafer-Level Packaging (WLP): WLP process standards — Identifies the need for standardized processes, materials definitions, and manufacturing expectations so that wafer-based packaging methods can be reliably adopted across suppliers and scaled up

HIR Chapter 24 Reliability: Reliability qualification standards — Highlights the importance of unified reliability guidelines (i.e., for covering materials, testing, data use, and system monitoring) so that all parts of increasingly complex electronic systems can be evaluated and supported consistently throughout their lifespan

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Key Gaps ("C#" indicates roadmap chapter)

- **Board-level attach lacks shared requirements:** No unified mechanical/electrical standards for very high pin counts [C22]
- **Inconsistent testing across device types:** RF, photonics, high-speed, and multi-chip devices need unified test methods [C17]
- **No common language for 2D/3D connections:** Industry lacks shared terms and metrics to describe chip-to-chip interconnects [C22]
- **No common SiP co-design data formats:** Multi-chip modules lack standardized design kits and data exchanges. [C21]
- **No shared criteria for ultra-fine pitch bonding:** There are no agreed limits for alignment, defects, or acceptance at very small pitches [C22][C23]
- **No standard panel sizes or processes:** Panel-level packaging uses inconsistent dimensions and handling rules that block scaling [C23]
- **No standards for passives embedded in packages:** Electrical quality and reliability expectations are undefined [C23][C21]
- **Outdated "one-size-fits-all" reliability qualification:** Current test suites don't reflect heterogeneous integration realities [C24]
- **Prognostics and health management (PHM) (health monitoring) is not standardized:** Sensors, telemetry, and aging models vary widely by vendor [C24] [C17]
- **Thermal modeling/measurement lacks alignment:** No shared guidance for stacked devices or self-heating effects [C24][C21][C23]

Key Opportunities/Recommendations ("C#" indicates roadmap chapter)

- **Adopt reliability qualification based on physics and data:** Tailor stress methods using shared responsible practices / AI guidelines instead of fixed test suites [C24]
- **Align thermal measurement and model validation practices:** Provide shared rules for evaluating heat behavior in stacked devices [C24][C21][C23]
- **Create a shared vocabulary for 2D/3D packaging:** Define simple, consistent terms and metrics for interconnect choices [C22]
- **Define board-level attach requirements for high pin counts:** Standardize mechanical/electrical expectations for dense interfaces [C22]
- **Develop shared SiP design kits and data formats:** Standardize the information needed to co-design multi-chip modules [C21][C24]
- **Issue guidelines for passives embedded in packages:** Specify electrical and reliability criteria for in-package passives [C23][C21]
- **Publish unified test methods across device classes:** Provide common approaches for RF, photonics, high-speed, memory, and multi-chip testing [C17]
- **Set acceptance criteria for ultra-fine pitch bonding:** Establish clear limits for alignment, defects, and performance at tiny pitches [C22][C23]
- **Standardize panel-level packaging:** Agree on panel sizes, handling rules, and process expectations to enable scaling [C23]
- **Standardize PHM building blocks:** Define sensors, telemetry, and aging models for consistent health monitoring [C24][C17]

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SRC MAPT Microelectronics & Advanced Packaging Technologies Roadmap [296]

Semiconductor Research Corporation (SRC), 2023

Focus

The MAPT roadmap provides a comprehensive, industry-wide plan for advancing U.S. leadership in microelectronics by integrating progress across devices, architectures, packaging, materials, sustainability, security, and workforce development. It extends the SRC / Semiconductor Industry Association (SIA) "2030 Decadal Plan" by translating the five major seismic shifts in semiconductors—smart sensing, memory/storage growth, communication bottlenecks, security challenges, and compute-energy limits—into detailed research priorities and technology strategies. The document recognizes that classical transistor scaling is no longer sufficient and future progress will rely on advanced packaging, heterogeneous integration, new compute paradigms, and a holistic, sustainability-driven ecosystem.

Goals

- Create a unified roadmap for heterogeneous integration (HI), 3D packaging, chiplet-based architectures, and system-technology co-optimization
- Achieve 1000× to 1,000,000× improvements in computing energy efficiency over ~20 years, aligning with DOE's EES2 effort
- Build a resilient, secure, and sustainable U.S. microelectronics ecosystem—from materials to manufacturing to end-of-life
- Strengthen national competitiveness by building a skilled, diverse workforce, aligned with industry-validated knowledge/skill frameworks
- Expand advanced packaging capacity to keep system-level innovation domestically owned and secure

Challenges/Barriers:

- **Data movement bottlenecks:** Memory bandwidth, interconnect energy, and latency now dominate system performance limits
- **Materials and manufacturing constraints:** Need for new substrates, interconnects, TIMs, dielectrics, bonding processes, and reliable 2.5D/3D integration flows
- **Security vulnerabilities:** New attack surfaces created by chiplets, multi-die integration, MEMS/analog components, supply-chain complexity, and in-field lifecycle exposures
- **Standards gaps:** Lack of common frameworks for chiplet interfaces, environmental metrics, 3D metrology, security, and quality across the supply chain
- **Sustainability pressures:** Rising greenhouse gas (GHG) emissions, water use, PFAS reliance, complex chemistries, and high resource intensity of advanced nodes
- **Thermal management:** High-density 3D stacks, chiplet systems, and power-hungry AI workloads require new cooling architectures and materials
- ***Workforce shortages:*** Large gaps in microelectronics-specific training, Science, Technology, Engineering, and Mathematics (STEM) pipelines, and advanced manufacturing talent

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Opportunities/Recommendations
- **Advance next-generation chip packaging:** Use new ways of connecting and stacking chips so they run faster, use less energy, and are easier to update or customize
- **Build sustainability into the whole lifecycle:** Reduce water use, emissions, and harmful chemicals; improve recycling; and design components that are easier to repair, reuse, or safely retire
- **Develop new kinds of computing:** Explore approaches beyond traditional processors—such as memory-focused designs, specialized accelerators, and other energy-saving computing models—to handle growing AI and data needs
- **Grow and modernize the workforce:** Expand training, education, and career pathways so more people can enter microelectronics, advanced packaging, and semiconductor manufacturing
- **Improve security in a multi-chip world:** Strengthen trust and protection across chiplets, packages, tools, and supply chains so that devices remain reliable and secure from design through deployment

Summary Report: CHIPS R&D Program Standards Summit [297]

NIST, 2023

Focus
Summarizes an inaugural Standards Summit (September 2023, led by NIST's CHIPS R&D Office); the Summit convened to accelerate private-sector-led semiconductor standards development as part of the CHIPS for America R&D program, and aligns with CHIPS Act mandates and the U.S. National Standards Strategy for Critical & Emerging Technologies.

Goals
By 2030, aims to strengthen U.S. semiconductor technology leadership, fast-track commercialization of innovations, and cultivate a robust domestic microelectronics workforce

Strategic Priorities
Identifies five high-priority standards areas for near-term focus: chiplets, data interoperability, digital twins, supply chain security & resilience, and advanced packaging & heterogeneous integration

Challenges/Barriers
- **Fragmented standards landscape:** Large number of overlapping standards across many SDOs complicates discovery and coordination
- **Standards pace vs. innovation:** Risk of standards being introduced too early (constraining innovation) or too late (hindering interoperability)
- **Participation barriers:** Small and medium enterprises (SMEs), startups, and researchers face cost, time, and process barriers to sustained standards engagement
- **Research–standards misalignment:** Pre-standards research and metrology are not always well-timed to inform standards development

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Opportunities/Recommendations
- **Standards incubators and accelerators:** Use new models to mature early standards ideas and speed transition into formal SDOs
- **Stronger SDO coordination:** Improve collaboration across standards bodies to reduce duplication and improve interoperability
- **Standards readiness metrics:** Develop readiness-level concepts to guide when technologies are suitable for standardization
- **Improved standards navigation tools:** Create shared tools to map, search, and understand standards and dependencies

The Decadal Plan for Semiconductors [298]

Semiconductor Research Corporation, 2021

Focus
The Decadal Plan outlines a strategic vision for semiconductor research and innovation over the next decade, identifying five seismic shifts that will transform the industry and Information and Communication Technology (ICT): analog electronics, memory and storage, communication, hardware-enabled security, and energy-efficient computing.

Goals
- Address emerging security challenges in highly interconnected systems and AI through hardware-enabled ICT security
- Develop radical new memory and storage technologies to overcome Si supply limitations and meet exponential data growth
- Discover new computing paradigms that offer orders-of-magnitude improvements in energy efficiency
- Drive fundamental breakthroughs in analog hardware to enable smarter sensing and reasoning capabilities
- Innovate communication technologies to handle the imbalance between data generation and transmission capacity, including 5G/6G and beyond

Challenges
- Growing energy demands outpacing global energy production
- Increasing complexity and heterogeneity in system architectures
- Need for new materials, devices, and architectures to sustain innovation
- Physical scaling limits in CMOS and traditional semiconductor technologies
- Security vulnerabilities introduced by new AI and quantum computing technologies
- Recommendations:
- Emphasize co-design of hardware and software, including AI and quantum computing integration
- Foster public-private partnerships to accelerate innovation and commercialization
- Increase federal investment by $3.4 billion annually to support multidisciplinary research

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Gaps and Emerging Needs

This section identifies areas where semiconductor standards are lacking, insufficient, or not yet put in place. These gaps span the entire spectrum of semiconductors. Gaps were identified through analysis of government reports, industry analysis, existing standards, academic research, and stakeholder inputs.

AREAS LACKING STANDARDS

Absence of standards for advanced packing reliability and thermal management: [299, 300, 301, 302, 303] Heterogeneous integration (HI) and chiplet-based designs create complex thermal paths and stress conditions that current single-die metrics do not address. There is no consensus standard for multi-die thermal modeling, test vehicles, or reliability criteria under realistic workloads. Industry roadmaps highlight missing elements including die–package–system co-design requirements, model exchange formats, standardized thermal verification flows, stress/warpage acceptance bands, power and thermal co-sign-off, and lifecycle reliability benchmarks. Recent studies show unmitigated 3D stacks can exceed 140°C, meaning there is a need for uniform test conditions, reporting, and mitigation benchmarks to ensure safe adoption.

Inadequate standards for emerging 2D semiconductor materials: [304, 305, 306] The rapid adoption of two-dimensional (2D) semiconductor materials, such as graphene and transition metal dichalcogenides (TMDs), is exposing major gaps in existing standards. Traditional norms designed for bulk Si do not address the unique properties, fabrication methods, or integration requirements of atomically thin materials. ISO and ASTM have introduced preliminary specifications for graphene characterization, but these efforts remain fragmented and fail to cover device-level performance metrics, reliability testing, and scalable manufacturing processes. Commercialization and interoperability across global fabrication facilities will continue to struggle in the absence of comprehensive standards for metrology, material purity, defect characterization, and integration protocols.

Inadequate standards for quantum-ready and post-CMOS integration: [307, 308, 309, 310, 311] Quantum and post-CMOS devices (e.g., spin qubits, photonics) are beginning to integrate with traditional CMOS processes. However, no industry-wide standards exist for thermal, electrical, signal integrity, or packaging compatibility in these hybrid systems. Each research group or startup uses proprietary methods for probe design, cryogenic control circuits, or optical packaging. Agreed-upon formats and interfaces are necessary to reduce the challenges associated with scaling these systems reliably and reproducibly. Standardized integration rules and traceable workflows would help bridge classical and emerging quantum hardware at scale.

Lack of comprehensive standards for chiplet interoperability across multi-chiplet systems: [312, 313, 14] Chiplet-based architectures are reshaping semiconductor design and enabling heterogeneous integration and advanced packaging. UCIe provides a foundation for physical and die-to-die connectivity, but current standards do not address higher-level interoperability for multi-

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chiplet systems, software integration, or management protocols. UCIe 1.1 and 2.0 remain focused on single die-to-die links, leaving gaps for complex multi-chiplet configurations and cross-vendor compatibility. This lack of comprehensive standards limits true plug-and-play functionality and creates fragmentation across market segments, where data center applications prioritize high bandwidth while consumer markets value cost and reusability. Developing layered standards for chiplet interoperability—including management, security, software integration, power and thermal management, error handling, and compliance testing—will be critical for scaling this design paradigm.

Lack of standards for AI-driven semiconductor design and verification:[315, 316, 317, 318] AI tools are now widely used to speed up chip design and improve efficiency. Yet, there are no clear standards for how these AI-generated results should be checked and documented. Key areas like data source tracking, reproducibility, transparency of AI decisions, and fallback options are not covered by existing verification standards. Today, companies rely on their own rules, which makes results inconsistent. A common standard could set guidelines for what evidence to keep, how to test AI-generated layouts, and how to ensure results can be reproduced across different tools.

Lack of standards for security in hardware IP and design tools: [319, 320, 321, 322, 323, 324] Hardware IP blocks and EDA tools are increasingly exposed to threats like malicious IP, supply chain tampering, and side-channel attacks. Although standardization consortia (e.g., Accellera) have proposed IP Security Assurance (SA-EDI) frameworks, these are not yet widely implemented or formally standardized. Companies therefore rely on inconsistent internal policies that increase vulnerability for IP integration and verification. A strong standard could define verification metadata, secure IP packaging, tamper-resistant annotations, and toolchain certification to enhance trust across the semiconductor ecosystem.

Missing standards for secure, trusted, and traceable supply chains:[325, 326, 327, 328, 329] There is no harmonized global framework for end-to-end traceability and provenance, and no widely adopted standards for digital certificates, unique hardware identifiers such as Physically Unclonable Function (PUF)-based or watermarking techniques, component pedigree documentation, or immutable device IDs. These tools help prevent counterfeiting, tampering, and gray-market infiltration. Chiplets and multi-die systems are on the rise, which further complicates vendor trust and supply chain transparency. Formal standards are needed to help companies ensure authenticity across third-party fabrication, packaging, test houses, and system integrators. Digital certificates are a possible solution but require buy-in from governments, manufacturers, and assembly houses. Broad industry consensus is required to define authentication protocols, data exchange schemas, and verification frameworks that can support national security, regulatory compliance, and market assurance.

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Missing standards for sustainability and environmental impact metrics: [330, 331, 332, 333, 334, 335] Semiconductor fabs consume vast amounts of water, energy, and chemicals. Individual practices exist, but no unified standard defines how to measure and report these impacts consistently across facilities. Metrics like electricity per wafer, ultrapure water (UPW) usage, carbon emissions, and chemical discharge vary by region and company. Without shared benchmarks and reporting protocols, it is difficult to compare sustainability performance, set meaningful targets, or ensure transparency. A semiconductor-specific standard could require uniform KPIs, measurement methods, and third-party verification to support environmental goals and stakeholder trust.

GENERAL/CROSS-CUTTING CHALLENGES

Challenges in sourcing raw materials and packaging: Many materials used to manufacture semiconductors are available globally; however, some essential raw materials such as gallium, germanium, copper, and tungsten are concentrated in a few locations around the world. This leaves producers dependent on these locations despite some being geopolitically sensitive.[336]

Elevated labor costs in the United States: A major factor in fab construction costs in the United States versus other countries is the cost of labor. In the United States, labor costs required for a fab are typically four or five times more expensive on a per-hour basis than in Asia. In Europe, labor costs are about two to three times more expensive than in Asia.[337]

Geopolitical tensions and export controls: Geopolitical unrest, conflicts, and escalating restrictions on semiconductor technologies and raw materials are reshaping semiconductor supply chains and the global competitive landscape of the industry. The United States, Japan, Netherlands and other countries have implemented export controls to restrict China's access to advanced semiconductors and the materials needed to produce them. This blocks Chinese firms from acquiring critical emerging technologies such as high-end chips and electronic design automation (EDA) software. Following this, in December 2024, China banned the export of critical minerals such as gallium, germanium, and antimony to the United States.[338] Overall, geopolitical unrest may disrupt semiconductor supply chains and exacerbate labor and supply shortages.

Global logistics constraints and infrastructure gaps: Logistical infrastructure is critical to the on-time delivery of materials that enable ongoing operations. Of the top 20 ports globally, there are only two in the United States and three in Europe. Additionally, the total volume handled by the ten largest U.S. ports is only 27% of the volume handled by China's ten largest ports.[339] These disparities affect cost control measures and extend shipping times for U.S. and European markets, further intensifying global supply chain inefficiencies.

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High capital and operating cost structures: The Bipartisan Infrastructure Law, the CHIPS Act, the Inflation Reduction Act, and state-specific incentives have encouraged rebuilding manufacturing and supply chain operations in the United States. Other countries have implemented similar incentives to regionalize semiconductor manufacturing. However, up-front capital and long-term operating costs for front-end capacity such as advanced logic fabs, materials, packaging, and other segments are higher in the United States relative to other regions such as China, Southeast Asia, and Taiwan.[340] AI has disproportionately driven investment and demand toward a few suppliers and distributors, which has boosted pricing power and profitability for leading companies.

Increasing material intensity in advanced manufacturing: Leading-edge chips and advanced packaging (AP) require increasingly complex manufacturing methods and increase the amount of materials needed to produce the final product. In the United States and Europe, investments primarily focus on developing more advanced manufacturing, rather than semiconductor materials. This may lead the United States and Europe to increase their reliance on Asia to provide basic and specialty materials.[341]

Large-scale investment requirements and uncertain returns: The CHIPS Act, as well as tax and trade policies from both the Biden and Trump administrations, have helped encourage domestic semiconductor manufacturing. The CHIPS Act allocated nearly $53 billion to support the semiconductor market, of which $39 billion was specifically designated for chip manufacturing and research. Following the CHIPS Act, nearly an additional $450 billion in private investments was announced across 28 states to increase domestic manufacturing capacity.[342] Despite large investments, capital is not always sufficient. Producing semiconductors requires timely and effective shipments of many chemicals and materials. The U.S. semiconductor industry is expected to almost double in value to $140 billion by 2030, leaving serious gaps as there is not enough domestic supply of materials to meet that level of demand.[343] This leaves investors facing uncertain returns on investments, which could hinder future investments and innovation.

Workforce and talent shortages: The United States faces a significant shortage of technicians, computer scientists, and engineers, with a projected shortfall of 67,000 workers in the semiconductor industry by 2030.[344] Workforce shortages stem from high attrition and an aging workforce. Companies will need to prioritize seizing talent, improve their employee value proposition, and shift skills in their existing workforce to stay competitive.

GAPS REQUIRING PRE-STANDARDIZATION R&D

Advancing metrology for complex 3D structures: [345, 346, 347, 348, 349, 350, 351]
Through-silicon vias (TSVs), nanosheets, and multi-die packages are complex 3D structures that are extremely difficult to measure using current metrology tools.

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Non-destructive defect detection, buried interface characterization, and hybrid metrology integration remain unresolved gaps. Other gaps include chemical mapping at nanometer scale and in-line metrology for emerging memory devices. Addressing these needs would enable new standards for 3D structure measurement, calibration protocols for hybrid metrology systems, and updates to reliability test standards for advanced packaging technologies.

Detecting and controlling emerging contaminants in wastewater:[352, 353, 354, 355, 356, 357] Semiconductor wastewater streams often contain PFAS, triarylsulfonium (TPS) salts, diaryliodonium compounds, azoles, and other trace organics that current analytical methods cannot reliably detect or remove. Corrosive and fouling conditions cause issues for monitoring. Point-of-use recycling technologies remain immature. Addressing these barriers would support new metrology standards for contaminant detection, interlaboratory test methods for PFAS removal, and updates to process water quality standards to ensure compliance and operational safety.

Developing energy-efficient and low-impact brine management solutions: [358, 359, 360, 361, 362, 363] Brine streams with high salinity and chemical complexity are a major problem for sustainable disposal and treatment. Existing technologies are energy-intensive, carbon-heavy, and often incompatible with emerging regulatory requirements. Solutions would enable new or revised standards for brine concentration and segregation methods, performance benchmarks for low-carbon treatment technologies, and revisions to facility discharge guidelines. Additional opportunities include defining best practices for preconcentration, alternative evaporation methods, and integrated brine recovery systems.

Enabling data interoperability and digital twin use integration in semiconductor manufacturing:[364, 365, 366] Semiconductor manufacturing and supply chain data remain fragmented across tools and organizations that lack common standards for data exchange. This hinders the deployment of integrated digital twin simulations across different facilities. Addressing this gap would enable new standards for data interoperability and digital twin integration.

Ensuring reliability and interoperability in chiplet and heterogeneous integration: [367, 368, 369, 370, 371, 372, 373] Multi-die packaging introduces challenges in thermal, mechanical, and corrosion reliability, as well as interoperability across vendors. Adoption is hindered by the lack of standardized testing and validation protocols for both die-to-die connections and overall system performance. Industry needs standardized approaches for electrical, thermal, and mechanical validation, and interoperability frameworks for chiplet ecosystems. Solutions would support new standards for chiplet interoperability and stress testing protocols, and they could also lead to revisions to JEDEC and IEC reliability standards to reflect emerging architectures.

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Improving energy-efficiency and thermal management across advanced fabs:[374, 375, 376, 377, 378, 379] Energy consumption and heat generation in advanced fabs are rising sharply as device complexity grows. Current heat recovery systems are limited, and there are currently no standardized "green tool" design principles. Fabrication facilities need innovations in two-phase cooling, immersion cooling, heat pipes, and diamond-based thermal interfaces to manage extreme power densities. Progress here could lead to new standards for energy recovery systems and thermal performance metrics for process tools. Closing these gaps could also enable revisions to industry-wide facility energy efficiency guidelines.

Managing water and chemical sustainability:[380, 381, 382, 383, 384] Facility-wide water recycling and ultrapure water (UPW) reuse remain difficult to implement because they require precise segregation, advanced treatment, and purity assurance to avoid yield loss. Beyond water, fabs must also address chemical lifecycle management for acids, solvents, and slurries, reduce hazardous waste streams, and minimize emissions of high global warming potential gases. Tackling these issues would enable new standards for water reuse validation and chemical recovery processes. It would also enable revisions to environmental performance guidelines and facility-level sustainability metrics.

Metrology for high-precision, no-contact and inline measurements[385]: Metrology tools must evolve to keep up with smaller, faster, and more 3D semiconductor devices, while not damaging them. The industry needs accurate measurements at very small scales, such as nanometers and below. Modern chip sizes in nanometers leave almost no room for error, and small amounts of variance can significantly impact performance and yield of chips.

Strengthening supply chain traceability and security: [386, 387, 388] Globalized semiconductor supply chains face persistent risks related to provenance, authenticity, and counterfeit detection. Current traceability mechanisms lack consistency and scalability across vendors and regions. Addressing these issues would enable new standards for digital identifiers, blockchain-based traceability frameworks, and secure serialization practices. Additional opportunities include harmonizing certification processes and defining assurance protocols for multi-vendor chiplet assemblies. Revisions would also be necessary for existing supply chain security and cybersecurity standards.

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Ongoing and Emerging Standardization Efforts

This section highlights current initiatives and working groups that are actively developing or piloting semiconductor standards, and includes efforts by standards bodies, industry consortia, and public-private partnerships that are shaping the future of semiconductor governance, safety, and interoperability. The section also includes pre-standardization activities and draft standards that signal emerging areas of focus.

ACTIVE WORKING GROUPS

Automotive Electronics Council (AEC): [389, 390] The AEC sets qualification standards for electronic components used in harsh automotive environments. AEC was established by major automakers. They publish widely adopted specifications including AEC-Q100 for ICs and AEC-Q101 for discrete semiconductors; these documents define stress test qualification requirements, including electrostatic discharge (ESD) tests, latch-up tests, and endurance evaluations for non-volatile memory. Their standards are critical for automotive-grade chips used in advanced driver-assistance systems (ADAS), powertrain control, and infotainment.

Electrostatic Discharge Association (ESDA): [391, 392, 393] The ESDA is the only ANSI-accredited organization dedicated to developing standards for electrostatic discharge (ESD) control and electrical overstress (EOS) in electronics manufacturing environments. Their website claims they have published more than 70 documents including standards, test methods, and technical reports, which offer guidance for creating robust ESD control programs. ESDA's flagship standard, ANSI/ESD S20.20, defines requirements for establishing and maintaining ESD-safe environments, covering personnel grounding, workstation design, and compliance verification. ESDA also updates companion documents such as ESD TR53 and ESD TR20.20 to reflect evolving best practices. These standards are critical for preventing costly component failures [394] and ensuring reliability in sectors like semiconductors, aerospace, and defense.

The European Semiconductor Industry Association (ESIA): [395, 396] ESIA represents the European semiconductor industry, advocating for a sustainable business environment and enhancing the global competitiveness of the industry. Established in 1997, ESIA helps shape the agenda of the World Semiconductor Council (WSC) with international counterparts from China, Japan, Korea, and the United States. ESIA activities include a large range of issues across the regulatory framework, such as industrial competitiveness, R&D, environmental and safety compliance, protections for IP, and anti-counterfeiting. ESIA has 22 members including Bosch, Infineon, Intel, Micron, and Texas Instruments (TI).

IEC Technical Committee TC 47 (Semiconductors): [397, 398, 399] IEC TC 47 is the primary international committee responsible for developing standards for semiconductor devices and related technologies; its scope covers discrete semiconductors, integrated circuits (ICs), sensors, display devices, and microelectromechanical systems (MEMS). The committee addresses critical

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areas such as wafer-level reliability, package outlines, environmental testing, and device-specific test methods. TC 47 operates through multiple subcommittees, including SC 47A (ICs), SC 47D (Semiconductor Device Packaging), and SC 47F (MEMS), each managing specialized working groups on topics like heterogeneous ICs, power devices, and wide bandgap (WBG) technologies. IEC standards ensure interoperability, quality, and environmentally sound practices across global semiconductor supply chains.

IEEE Standards Association: [400] IEEE is a global standards development organization that contributes to semiconductor-related standards through multiple technical committees (TCs) and working groups. Their efforts span areas like IC reliability, hardware security, and emerging architectures. Active projects include standards for domain-specific accelerators, flexible and wearable electronics, and secure hardware frameworks. IEEE's work complements formal standards development by ISO/IEC and SEMI, ensuring alignment across global semiconductor ecosystems.

IPC (Association Connecting Electronics Industries): [401, 402] IPC develops standards for printed circuit boards (PCBs) and electronic assemblies, which are critical for semiconductor packaging and integration. Their widely adopted standards include IPC-7351 (land pattern design) and IPC/JEDEC J-STD-033 (component handling and storage). Broadly, IPC's work supports reliability and interoperability across electronic systems that incorporate semiconductor components.

ISO/IEC JTC 1 and related semiconductor-focused subcommittees: [403, 404] ISO/IEC JTC 1 is a joint technical committee focused on information technology standards, but its work intersects with semiconductor technologies through subcommittees on interconnection, security, and emerging technologies. For example, SC 25 develops standards for interconnection of IT equipment, which influences semiconductor interface requirements, while SC 27 addresses cybersecurity and privacy—critical for secure chip design. JTC 1 also manages working groups on cloud computing, IoT, and AI, all of which depend on semiconductor innovations. Although JTC 1 does not create device-level standards, its frameworks for interoperability and data exchange complement semiconductor standards from IEC and JEDEC, ensuring consistency across global ICT ecosystems.

Japan Electronics and Information Technology Industries Association (JEITA): [405, 406, 407] JEITA is a leading Japanese trade association that develops standards for electronics and IT industries. Its standards framework aligns with JIS Z 8301 [408] (i.e., the "rules for the layout and drafting of Japanese Industrial Standards [JIS]) and covers areas such as electromagnetic compatibility (EMC), connector interfaces, and reliability testing for semiconductor devices. JEITA standards are reviewed every five years to ensure relevance, with outcomes ranging from

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revisions to abolishment or confirmation. Recent initiatives include working groups on semiconductor EMC performance equivalence for stabilizing supply chains and improving productivity. They also play a role in harmonizing Japanese standards with international frameworks to support global interoperability.

Joint Electron Device Engineering Council (JEDEC) Solid State Technology Association: [409, 410, 411] JEDEC is a globally recognized SDO for microelectronics and focuses on memory interfaces, packaging, and reliability testing. Active committees include JC-11 (Mechanical Standardization), JC-14 (Quality & Reliability), JC-42 (Solid-State Memories), and JC-70 (Wide Bandgap Power Semiconductors). Current projects address next-generation DRAM (HBM4), LPDDR6, and advanced packaging standards for heterogeneous integration. JEDEC standards are widely adopted across the semiconductor supply chain to ensure interoperability and performance consistency.

National Electronics Manufacturing Initiative (NEMI): [412, 413, 414] NEMI—which now operates as iNEMI—is an industry-led consortium that focuses on advancing electronics manufacturing through collaborative roadmaps and standards development. NEMI's technology roadmaps identify gaps and guide investment in areas such as advanced packaging, factory integration, and sustainable electronics. Their NEMI projects have addressed interoperability challenges, including the "Plug and Play Factory" initiative, which developed infrastructure for integrating new assembly equipment into production lines. Today, iNEMI continues to influence global supply chain standards and best practices through technical working groups on topics like flexible hybrid electronics, MEMS, and smart manufacturing.

NIST Semiconductors and Microelectronics Standards Working Group (SMSWG): [415, 416, 417, 418] NIST chairs the interagency working group, SMSWG, under the U.S. National Standards Strategy for Critical and Emerging Technologies. This group focuses on advanced packaging, HI, chiplet interoperability, and sustainability metrics. NIST collaborates with ISO/IEC, IEEE, SEMI, and JEDEC to align U.S. priorities with international standards development and accelerate pre-standardization research.

SEMI International Standards Program: [419, 420, 421] SEMI coordinates one of the largest semiconductor standards programs globally, with more than 200 active task forces and committees. These groups develop standards for wafer specifications (e.g., SEMI M1, M76), equipment communication protocols (SEMI E6, E30), and advanced packaging technologies. SEMI standards are essential for fab interoperability and supply chain consistency, supporting manufacturing efficiency and global competitiveness.

The Semiconductor Industry Association in the United States (SIA): [422, 423, 424] SIA is the leading trade association representing the computer chip industry; it

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aims to provide leadership for U.S. chip manufacturing on critical issues of trade, technology, environmental protection, and worker safety and health to maintain U.S. leadership in technology. The SIA actively lobbies the U.S. Congress and the Executive Branch, advocating for policies—such as the CHIPS and Science Act—that strengthen domestic manufacturing and fund critical semiconductor research and development.

World Semiconductor Council (WSC):[425, 426, 427] The WSC is a global forum comprising semiconductor associations from six major regions: the United States, EU, Japan, Korea, China, and Chinese Taipei. WSC does not publish technical standards but does coordinate industry positions on standards-related issues, trade policy, and environmental health and safety initiatives. Recent WSC joint statements emphasize harmonization of standards, IP protection, and sustainability practices.

ACTIVE STANDARDS INITIATIVES

This section highlights significant ongoing initiatives that actively drive or accelerate standards development in semiconductors and microelectronics. These efforts include major government-funded programs, multi-stakeholder consortia, public–private partnerships, and other collaborative projects. They provide practical resources ranging from R&D funding and testbed infrastructure to demonstration projects and new coordination mechanisms, and act as catalysts for standardization progress in areas like manufacturing, design, supply chain security, and more. Active standards initiatives comprise strategic policy imperatives and formal standards development including notable government-backed programs (such as CHIPS for America R&D investments, the EU Chips Act's capacity-building efforts, etc.) and industry-driven consortia and projects that are collectively shaping the global standards landscape.

Creating Helpful Incentives to Produce Semiconductors (CHIPS) for America R&D Standards Program:[428, 429, 430, 431] NIST administers the CHIPS for America program, which invests $11 billion to strengthen U.S. leadership in semiconductor research and development. A key component is accelerating standards for advanced packaging, chiplet interoperability, cybersecurity, and metrology. NIST has emphasized the need for standards to keep pace with rapid innovation and to ensure interoperability across global supply chains. In September 2023, NIST convened the CHIPS R&D Standards Summit, which brought together different stakeholder groups including standards organizations to identify priorities and create an innovation-focused roadmap for semiconductor standards. The Summit emphasized linking standards to research, enabling agile development processes, prioritizing standards development for chiplets, data interoperability, digital twins, supply chain security and resilience, advanced packaging and HI, and building a diverse workforce capable of driving standards adoption.

European Chips Act / "Chips for Europe" Initiative:[432, 433, 434] The European Chips Act was introduced in September 2023 along with the "Chips for Europe"

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Initiative to boost EU sovereignty in semiconductor technologies. This initiative funds advanced pilot lines for sub-2nm process development, HI, and quantum chip research, and establishes a pan-European design platform and a network of competence centers to support standards harmonization and interoperability. The Initiative bridges research and industrial deployment with the goal of doubling Europe's global semiconductor market share to 20% by 2030.

OCP Compute/Chiplets Project/Open Chiplet Economy: [435, 436, 437] The Open Compute Project (OCP) is advancing an open vendor-neutral ecosystem (known as an "Open Chiplet Economy") for chiplet-based design and manufacturing. It builds on principles of modularity by enabling disaggregated Si components (chiplets) to be integrated into advanced 2D and 3D system-in-package (SiP) architectures. The initiative addresses both technical and business challenges by standardizing interfaces, design workflows, and collateral needed for multi-vendor interoperability. Recent contributions include the Foundation Chiplet System Architecture (FCSA), which defines a baseline framework for breaking down monolithic SoCs into smaller, reusable chiplets with standardized interfaces. This framework makes it feasible to integrate components from multiple vendors. Additionally, Bunch of Wires (BoW) 2.0 introduces enhancements for high-bandwidth, low-latency interconnects optimized for memory-intensive workloads such as AI and HPC, addressing scalability and power efficiency challenges in chiplet ecosystems. The OCP website explains that these efforts aim to reduce fragmentation, promote open specifications, and accelerate adoption of chiplet architectures across the semiconductor industry.

SEMI & Semiconductor Climate Consortium (SCC) Sustainability Standards Initiative: [438, 439, 440] The SCC, which was launched under SEMI, focuses on harmonization of sustainability standards for the semiconductor industry. Its Sustainability Standards Initiative is developing industry-wide frameworks to standardize GHG accounting and reporting across the semiconductor value chain. Current efforts include publishing guidelines for "Scope 3 emissions" to ensure consistency in data collection, boundary setting, and calculation methods. The standards intend to create uniformity in emissions reporting, improve transparency, and enable comparability across suppliers and manufacturers. To support global decarbonization goals and position the semiconductor industry to meet emerging regulatory requirements, the initiative introduces clear methodologies for evaluating/measuring lifecycle emissions and renewable energy adoption.

DRAFT STANDARDS

Several draft standards are currently under development to address emerging needs in semiconductor and microelectronics manufacturing. These draft standards focus on areas including smart manufacturing data governance, equipment cybersecurity, wafer specifications, and device reliability. The table below summarizes key draft standards currently in progress across major standards bodies.

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Standards Body	Draft Standard	Focus Area	Descriptive Title of Standard
IEC / DIN (CENELEC)	EN IEC 63287-3 [441, 442]	Device Reliability	Reliability Qualification Plans for Power Semiconductor Modules – Part 3
IEEE	IEEE P1450.1/D2 [443]	Semiconductor Test Interface	Extensions to Standard Test Interface Language (STIL) for Semiconductor Design
IEEE	IEEE P3405 [444, 445]	Chiplet Interconnect Test and Repair	Standard for Chiplet Interconnect Test and Repair
SEMI	SEMI MDD (e.g., Doc 6938C) [446, 447]	Smart Manufacturing / AI Data	Guide for Equipment Edge Data Governance
SEMI	SEMI S2 Revisions (e.g., S2-0825) [448, 449]	Environmental, Health, and Safety (EHS) Interlocks	Environmental, Health & Safety Guideline Revisions (safety interlock systems)
SEMI	SEMI 4624A[450]	Wafer Quality	Specification for 450 mm Polished Silicon Wafers
SEMI	SEMI 6506 [451, 452]	Equipment Cybersecurity	Cybersecurity Requirements for Fab Equipment

NATIONAL AND INTERNATIONAL STRATEGIES

This section provides an overview of national and international strategies that influence semiconductor and microelectronics standardization. These strategies outline policy frameworks, investment priorities, and collaborative initiatives that shape technology development, supply chain resilience, and standards alignment across global ecosystems.

United States

CHIPS and Science Act of 2022:[453, 454, 455] The CHIPS and Science Act is a landmark U.S. initiative aimed at revitalizing domestic semiconductor manufacturing, research, and workforce development; it authorizes $52.7 billion for semiconductor-related programs, including $39 billion for manufacturing incentives and $11 billion for R&D through the Department of Commerce's CHIPS Program Office and CHIPS R&D Office. Key components include the establishment of the National Semiconductor Technology Center (NSTC), the Microelectronics Commons, and funding for advanced packaging, HI, and secure hardware architectures. The Act also supports standards development by promoting voluntary consensus-based approaches and aligning U.S. priorities with international standards bodies such as ISO/IEC and IEEE.

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Executive Order 14017 – America's Supply Chain: Signed in 2021, this executive order launched a government-wide initiative to strengthen U.S. supply chain resilience in response to COVID-19 disruptions and rising geopolitical risks. It identified semiconductors as one of four priority sectors and directed the Department of Commerce—alongside agencies including the Departments of Defense and Energy—to conduct a 100-day review and subsequent deep-dive assessments of semiconductor supply chains. These reviews identified key vulnerabilities, including geographic concentration in advanced manufacturing and gaps in domestic capabilities, and helped inform subsequent policies such as the CHIPS and Science Act and related microelectronics initiatives.[456]

National Strategy on Microelectronics Research:[457] The NSTC Subcommittee on Microelectronics Leadership released the *National Strategy on Microelectronics Research* in 2024, which provides a framework for advancing U.S. leadership in semiconductor R&D under the CHIPS and Science Act. The strategy identifies four core goals: 1) fuel discoveries for next-generation microelectronics, 2) expand and train the domestic workforce, 3) accelerate lab-to-fab infrastructure and technology transition, and 4) strengthen supply chain security through coordinated federal investments. The strategy focuses on pre-standardization research in areas such as advanced packaging, HI, and secure hardware architectures; promotes collaboration among federal agencies, industry, academia, and international partners; and calls for leveraging user facilities and public-private consortia to ensure rapid commercialization and standards alignment.[458, 459]

China

International partnerships:[460, 461, 462] China's partnerships increasingly center on AI-driven semiconductor technologies. Despite U.S. export controls, Chinese firms like Huawei and Alibaba are advancing AI chip design and large-scale models; they are supported by state-led R&D and Big Fund III investments in 3D integration and advanced packaging.

Manufacturing Leadership and Infrastructure

- China is the world's largest electronics manufacturing hub, producing 36% of global electronics and accounting for 42% of global semiconductor equipment spending in 2024, the highest worldwide.[463, 464] China's semiconductor ecosystem is organized under a "3+2" regional model, with Beijing, Shanghai, and Shenzhen serving as logic chip hubs anchored by firms like Semiconductor Manufacturing International Corporation (SMIC), Huahong, and Huawei, while Wuhan and Hefei specialize in memory production through leaders such as Yangtze Memory Technologies Corp. (YMTC) and ChangXin Memory Technologies (CXMT).[465, 466, 467]

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– China is advancing in semiconductor manufacturing by improving capabilities in advanced nodes and mature processes while strengthening its domestic equipment sector in areas such as etching, deposition, photolithography, ion implantation, chemical-mechanical polishing (CMP), wafer testing, and wafer cleaning. Regional industrial clusters integrate fabrication facilities, universities and vocational training centers, electronic design automation (EDA) design houses, R&D centers, and suppliers to accelerate technology transfer and achieve economies of scale.[468, 469, 470, 471, 472]

Roles in standards development:[473, 474, 475, 476, 477] China has evolved from a standards adopter to a global leader; they currently hold leadership positions in ISO and IEC TCs and have contributed to over 180 international standards since 2015. The Standardization Administration of China (SAC) represents China in ISO and IEC and coordinates international cooperation; it oversees 92 TCs and 780 secretariats.

– During the 2025 Qingdao Forum on International Standardization, ISO and IEC leaders highlighted China's role as the top country in ISO participation; Chinese experts were reportedly involved in 99% of TCs, leading 10% of them. China has published 2,484 foreign-language editions of national standards, spanning sectors from robotics to AI.

Self-reliance national strategy and funding:
China's Semiconductor Strategy within Five-Year Plan Framework:[478, 479, 480] China's semiconductor strategy is embedded in its 14th Five-Year Plan (2021–2025) and related industrial policies. The strategy's goal is to achieve technological self-reliance and global competitiveness through five key priorities: 1) advancing logic process nodes toward 7nm and 5nm production, 2) scaling memory technologies including NAND, DRAM, and HBM, 3) breakthroughs in lithography and packaging, 4) localization of core equipment, materials, and subsystems, and 5) development of domestic EDA tools to enable a self-reliant design ecosystem. The plan also calls for strengthening industrial clusters in Beijing, Shanghai, and Shenzhen, and expanding capacity for memory hubs in Wuhan and Hefei. China's approach integrates standards development into its broader innovation agenda. The action plans described in the strategy seek to accelerate standardization for ICs and advanced computing chips. The upcoming 15th Five-Year Plan (2026–2030) will prioritize breakthroughs in 7nm/5nm logic nodes, memory scaling (including HBM), lithography, and localization of core equipment and EDA tools.

Investments: [481, 482, 483, 484] China's National Integrated Circuit Industry Investment Fund ("Big Fund III"), valued at 344 billion yuan (~$47.5 billion USD), is channeling resources into advanced packaging and 3D integration technologies to bypass U.S. export restrictions and accelerate AI chip development. China has totaled about 686.6 billion yuan (~95.7 billion) in stake-backed investment funds since 2014 to expand domestic fabrication capacity and secure supply chains.

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Semiconductors as top industrial priority: [485, 486, 487] China has designated semiconductor chip development as a top industrial priority of its broader technological self-reliance agenda. The government launched the Made in China 2025 initiative to reduce foreign dependency and set targets for domestic chip production—40% by 2020 and 70% by 2025.

Subsidy strategy: [488, 489] China recently (2025) introduced a "precision-driven" subsidy strategy that, instead of providing blanket incentives, shifts to targeted funding for critical gaps such as high-end lithography, advanced packaging, EDA software, semiconductor manufacturing equipment, inspection and metrology systems, and specialized semiconductor materials. This approach centers on performance audits and collaboration between public institutions and private enterprises to ensure measurable technological progress.

Workforce development: [490, 491, 492] China's workforce strategy aims to build a domestic talent pipeline for semiconductor R&D and manufacturing. It calls for partnerships with global universities and promotes STEM education to close skill gaps.

– Rapid fab expansion has created acute talent shortages in lithography, wafer processing, and advanced packaging. Universities and vocational schools are expanding microelectronics programs, but supply lags demand. SEMI and the Ministry of Industry and Information Technology (MIIT) have launched workforce development forums to address these gaps through industry-academic collaboration.

European Union

Innovation ecosystem and infrastructure

Chips for Europe Initiative and Chips Joint Undertaking (Chips JU): [493, 494] Under the European Chips Act, the Chips for Europe Initiative establishes advanced pilot lines, a pan-European design platform, and a network of competence centers to accelerate the transition from R&D to manufacturing. These efforts are implemented through the Chips JU: a large-scale public-private partnership that manages multi-billion-euro investments and integrates standards harmonization into Europe's semiconductor innovation ecosystem.

Competence Centers Network: [495] The EU's competence centers network provides access to design tools, prototyping facilities, and guidance on emerging standards, particularly supporting SMEs and startups. These centers contribute to pre-standardization research in areas such as advanced packaging, HI, and secure hardware architectures.

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Standards development role

European Chips Act (EU): [496, 497, 498] The European Chips Act (2023) aims to double Europe's global semiconductor market share to 20% by 2030 and strengthen technological sovereignty. There are three pillars: 1) the Chips for Europe Initiative to fund pilot lines for advanced nodes and packaging, 2) a framework to incentivize public-private investments in fabs and R&D, and 3) a coordination mechanism through the European Semiconductor Board for crisis response and standards alignment. The Act emphasizes interoperability and resilience, and supports standardization for advanced packaging, secure hardware architectures, photonics and optoelectronics, wide-bandgap (WBG) semiconductors (like SiC and GaN), HI, and secure supply chains.

European Semiconductor Industry Association (ESIA): ESIA is Europe's principal industry association for semiconductors; it represents the region's leading chipmakers and suppliers and advocates for a competitive, sustainable semiconductor ecosystem in Europe. ESIA engages with EU policymakers on regulatory frameworks (e.g., R&D incentives, IP protection, anti-counterfeiting) to strengthen industry growth and supply chain resilience. ESIA also plays a global coordination role in setting the European agenda within the World Semiconductor Council (WSC), working with international counterparts (from the United States, Japan, China, Korea, etc.) to harmonize standards and best practices worldwide.

Global standards alignment: [499] The EU engages in international standardization to align European standards with global frameworks, reduce duplication, and promote interoperability. The EU also employes formal cooperation mechanisms (such as the Vienna agreement between CEN and ISO, and the Frankfurt Agreement between CENELEC and IEC) to enable coordination between European standards and international standards developed through SDOs like ISO and IEC.

Strategic coordination of standards: [500, 501, 502] The EU acts as a strategic policy and coordination hub for semiconductor and microelectronics standardization and aligns the work of European standards development organizations with EU objectives such as digital sovereignty, supply chain resilience, and technological competitiveness. The EU supports harmonized approaches through coordination with CEN, CENELEC, and ETSI that promote interoperability and consistency across the European market.

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India

Innovation ecosystem and infrastructure [503, 504, 505]

Emerging regional clusters: India is rapidly establishing several semiconductor clusters that aim to replicate global models like Silicon Valley and U.S. manufacturing hubs that essentially promote integrated ecosystems that span from R&D to production.

Value chain development: India is simultaneously scaling wafer fabs, chip packaging and testing facilities, and design centers, thereby creating an integrated ecosystem that reduces reliance on imports, supports domestic innovation, and attracts global players to establish advanced manufacturing capabilities within India.

International partnerships [506, 507]

Tata–Intel strategic alliance: In December 2025, Tata Electronics signed a Memorandum of Understanding (MOU) with Intel to support chip and packaging manufacturing in India, reinforcing the domestic supply chain and integrating global chipmakers into India's fast-growing ecosystem.

U.S.–India supply chain collaboration: Under the U.S. Department of State's International Technology Security and Innovation (ITSI) Fund (CHIPS Act), India Semiconductor Mission (ISM) partners to evaluate and strengthen workforce, regulatory, and infrastructure capabilities—laying the groundwork for future joint programs.

National strategy and funding

Fabrication and design incentives: [508, 509] The Semicon effort provides up to 50% financial support for establishing Silicon CMOS fabs, display plants, compound semiconductor fabs, and Outsourced Semiconductor Assembly and Test (OSAT) / Assembly, Testing, Marking, and Packaging (ATMP) [510] units. Semicon also comprises the Design Linked Incentive (DLI) Scheme, which provides 50% reimbursements for startup design costs for SMEs.

India Semiconductor Mission (ISM): [511, 512, 513] India launched its $10 billion initiative ISM to build a full-stack semiconductor ecosystem, including fabs, ATMP units, and DLIs. The next phase of the roadmap, ISM 2.0, was announced in 2025, and described a goal of making India a "product nation." It calls for shifting from fabs to advanced packaging, chip design, and R&D. India's strategy includes partnerships with global firms and participation in international standards bodies to ensure interoperability and trusted supply chains.

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Semicon India Programme: [514, 515] India launched its semiconductor strategy in 2021 with a ₹76,000 crore (or roughly ~$10 billion USD, based on the exchange rate at that time) investment package.The Semicon program established the ISM as the implementing agency with the goal of enabling end-to-end capabilities in chip and display manufacturing through capital support and global technology collaborations.

Role in standards development

Active national standards participation: [516, 517, 518] India's Bureau of Indian Standards serves as the national standards body and represents India in global forums such as ISO, IEC, Pacific Area Standards Congress (PASC), and the South Asian Regional Standards Organization (SARSO). BIS contributes to over 400 ISO TCs and holds secretariat roles in multiple working groups. BIS provides overarching governance for industrial and ICT standards and works alongside the Telecommunication Engineering Centre (TEC)—the technical arm of the Department of Telecommunications—which focuses on telecom and ICT standards. Both BIS and TEC coordinate to harmonize India's standards with global norms in support of the microelectronics and semiconductors industry sector.

Coordination with IEEE standards: [519, 520, 521, 522, 523] TEC collaborates closely with IEEE through a formal cooperation program that allows for India to adopt and adapt IEEE standards for national use. Senior TEC officials participate in IEEE-SA Standards Board activities and Government Engagement Program workshops; BIS provides overarching policy alignment for these adoptions. BIS and TEC also co-host IEEE-industry events (e.g., ITC India) to strengthen India's role in global standards development.

Workforce and talent

Expanding talent pipeline: [524, 525] India's semiconductor sector is creating significant demand; estimates suggest there are ~220,000 current professionals with projected shortfalls of 320,000–350,000 skilled roles by 2026 in areas spanning Very Large-Scale Integration (VLSI) design, fabrication, packaging, and testing. To meet rising budgets and production targets, the country aims to train 500,000 additional specialists annually, including engineers, technicians, and quality experts.

Specialized VLSI capabilities: [526, 527, 528, 529] VLSI involves embedding millions-to-billions of transistors on a single chip—this is applicable to modern ICs such as AI accelerators, IoT sensors, and mobile processors. India has 250,000–300,000 VLSI engineers that represent ~20% of the global IC design workforce. VLSI growth stems from Indian Institutes of Technology (IIT)-certified curricula and industry-driven programs (e.g., C2S), strengthening mid-to-senior leadership in VLSI roles through 2030.

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Training initiatives:[530, 531, 532, 533, 534, 535] India's Chips to Startup (C2S) program aims to develop 85,000 engineers in VLSI and embedded systems across more than 100 institutions. The initiative leverages IIT-based Centers of Excellence and the C-DAC's ChipIN facility to provide state-of-the-art EDA tools up to 5 nm node access, and includes public–private partnerships—such as Micron–IIT Delhi for AI-driven semiconductor modelling and Tata Electronics–Tokyo Electron Limited (TEL) / ASMPT collaborations—for hands-on chip design and fabrication R&D. IIT Centers of Excellence play a pivotal role by providing advanced design infrastructure and research capabilities; they enable hands-on experience with cutting-edge semiconductor tools and help to foster collaboration between academia and industry. India's training initiatives enhance practical skills in SoC design, EDA tool usage, and prototype tape-outs, and prepare mid-to-senior technical leadership roles through 2030.

Japan

Innovation ecosystem and infrastructure: [536, 537, 538, 539, 540, 541] Japan's semiconductor ecosystem comprises world-class materials suppliers, advanced equipment manufacturers, strategic design capabilities, dedicated workforce development programs, and newly established R&D hubs. Several Japanese companies dominate global markets for photolithography tools, Si wafers, semiconductor cleaning equipment, high-purity wet chemicals, CMP slurries and pads, and photoresists—all of which are critical inputs for advanced logic and memory chips. Japan has invested heavily in advanced packaging, HI, chiplet-based architectures, and optical SoC designs. Several new fabrication facilities and research facilities have received funding through priorities identified through Japan's *Semiconductor Revitalization Strategy;* they serve as testbeds for reliability benchmarking and packaging standards. Japan's infrastructure investments aim to position Japan as a global leader in semiconductor manufacturing while shaping standards for interoperability and sustainable production practices.

International partnerships: [542] Japan's semiconductor strategy relies on global partnerships that deliver tangible benefits, including joint development of 2 nm process technologies, advanced packaging standards, and supply chain risk monitoring systems. Collaborations with the United States, EU, and leading research hubs like IBM and Imec accelerate Japan's roadmap for chiplet integration, photonics-electronics convergence, and reliability benchmarking.

Japan–EU Digital Partnership Council: [543, 544] The Japan-EU partnership fosters cooperation on semiconductor R&D, sustainability standards, and workforce training. The agreement also supports harmonization of standards for advanced packaging and energy-efficient manufacturing practices.

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Japan's Semiconductor and Digital Industry Strategy (METI): [545, 546] Japan's "METI" strategy emphasizes three pillars: 1) strengthening domestic production capacity for IoT and industrial semiconductors, 2) establishing next-generation technologies such as 2 nm logic devices and advanced memory through Japan–U.S. collaboration, and 3) investing in future technologies like photonics-electronics convergence and optical chiplets. The strategy also prioritizes advanced packaging and chiplet integration, alongside stable access to critical materials and manufacturing equipment; promotes regional industry–academia consortia and global R&D cooperation; and aligns with Japan's broader economic security goals and includes significant public-private investment incentives, such as subsidies for advanced fabs operated by TSMC and Rapidus.

Rapidus partnerships: [547, 548, 549, 550] Japanese semiconductor manufacturer, Rapidus, has formed two major collaborations to accelerate Japan's semiconductor roadmap. With IBM, they develop 2 nm process technology and chiplet packaging that leverages IBM's Albany NanoTech Complex for advanced R&D and technology transfer. Separately, Rapidus joined IMEC's Core Partner Program, which provided them with access to global research infrastructure for photonics-electronics integration, advanced packaging standards, and reliability benchmarking.

U.S.–Japan Commercial and Industrial Partnership (JUCIP): [551, 552, 553] The JUCIP focuses on joint development of advanced semiconductor technologies, including 2 nm process nodes, advanced packaging, and secure supply chains. The partnership also promotes alignment on standards and workforce development, and addresses cybersecurity frameworks for semiconductor manufacturing environments.

Standards development role: [554, 555, 556, 557, 558, 559] Japan is an active participant in ISO/IEC JTC 1 for ICT and semiconductor-related standards. They also collaborate with IEEE and SEMI on semiconductor-specific standards including advanced packaging, chiplet integration, heterogeneous SoC architectures, Si photonics and co-packaged optics, thermal management and reliability benchmarking, energy-efficient interconnects, and cybersecurity guidelines for semiconductor manufacturing environments.

Japan Electronics and Information Technology Industries Association (JEITA): [560, 561, 562, 563] Japan's leading industry association, JEITA, coordinates domestic electronics and IT standards in alignment with Japanese Industrial Standards (JIS) (e.g., JIS Z 8301 formatting rules). JEITA's standards cover semiconductor-related areas like electromagnetic compatibility (EMC), connector interfaces, and reliability testing. These standards are reviewed on a ~5-year cycle to ensure they stay relevant (with updates, confirmations, or retirements as needed). Recent JEITA initiatives include working groups on semiconductor EMC performance equivalence to stabilize supply chains and boost productivity. JEITA also actively works to harmonize Japan's standards internationally.

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– Japan uses industry alliances and programs such as the Leading-Edge Semiconductor Technology Center (LSTC) to build a coordinated framework for next-generation semiconductor development that integrates research, manufacturing, and standards-setting. LSTC's mandate includes advancing 2 nm process technologies, developing chiplet-based architectures, and establishing reference designs and reliability benchmarks for advanced packaging. Japan's industry partnership reportedly focuses on sustainability standards, energy-efficient interconnects, and cybersecurity guidelines for semiconductor fabrication facilities.

Strategic framework and funding: [564, 565, 566, 567] Japan's Semiconductor Revitalization Strategy (2024) sets three pillars: 1) secure manufacturing infrastructure, 2) establish next-generation technologies, and 3) advance R&D for future innovations such as advanced logic and memory semiconductors. The plan targets mass production of 2 nm logic chips by 2027 and is supported by the LSTC. Japan has made unprecedented investments in R&D and chip production: ~$7B allocated for next-generation chip R&D and ~$4B for advanced chip production. These are part of a broader ¥10 trillion (~$64B USD) pledge through 2030.

Netherlands

International collaboration: [568, 569, 570, 571] The Netherlands is a founding member of the European Semicon Coalition with connects with other EU countries to coordinate semiconductor strategy under the EU Chips Act. The Coalition maintains a collective fund of €43 billion to support R&D, capacity building, and supply-chain resilience.

– The Netherlands also established bilateral cooperation through the Netherlands–New York State partnership, which promotes semiconductor R&D, student exchanges through the Eindhoven Semiconductor Summer School, and sustainable manufacturing innovations.
– The Netherlands is also expanding global engagement through Photonics and ICT collaboration with Taiwan in which Dutch companies and Taiwanese collaborate across design, packaging, module integration, and manufacturing

Semiconductor infrastructure and innovation ecosystem: [572, 573, 574] The Netherlands' semiconductor ecosystem encompasses world-leading equipment (ASML), front-end technologies (ASM International N.V.), packaging equipment (BESI), and design/manufacturing capabilities (NXP, Nexperia). The ecosystem is heavily concentrated in Brainport Eindhoven with support from over 300 deep-tech firms and a workforce exceeding 60,000 individuals. R&D hubs provide critical infrastructure for pilot production and standard setting in chiplet and heterogeneous integration.

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Standards development role:[575, 576, 577, 578] The Netherlands drives standards in extreme ultraviolet (EUV) and deep ultraviolet (DUV) lithography, atomic layer deposition (ALD) tools, metrology for inspection, hybrid packaging systems, and cleanroom process controls; its key industry leaders include ASML, ASM International N.V. (not to be confused with the U.S.-based professional society), and BESI.

– Two Dutch organizations serve as national hubs for semiconductor R&D and standards alignment: TNO and the ChipNL Competence Centre. These organizations have an explicit approach to pre-standardization through their coordination of multi-stakeholder projects involving industry, academia, and government to develop standards for chiplet architectures, HI, photonic packaging, energy-efficient interconnects, and sustainable production processes. [642, 643, 644, 645] Institutes co-develop photonic transceivers and packaging methods.

Strategic priorities and funding [579, 580, 581, 582]
Project Beethoven: The Netherlands made a €2.51B investment in Project Beethoven: a strategy for the Brainport Eindhoven region designed to strengthen the semiconductor ecosystem through housing, infrastructure, business climate improvements, and significant resources dedicated to talent development.

Export-control regulations: The Dutch government implemented export-control regulations on advanced semiconductor manufacturing tools including EUV/DUV lithography, ALD, epitaxy, and inspection equipment. These regulations aim to protect national security and maintain technological leadership by preventing sensitive technologies from being used in ways that could undermine global supply chain integrity.

Workforce development
ChipNL Competence Centre: [583, 584] The ChipNL Competence Centre is a €12 million effort that connects SMEs and startups with pilot lines and seeks to build expertise in integrated photonics, HI, and chip packaging. Its activities are tied to pre-standardization work through the development of shared design rules and packaging guidelines, which feed into European semiconductor standards frameworks.

University programs (e.g. University of Twente): [585, 586] Several Dutch universities have launched specialized semiconductor degree programs covering device fabrication, packaging, and sustainable microelectronics to build a future pipeline of highly qualified engineers.

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South Korea

International partnerships and workforce development:[587, 588, 589, 590, 591, 592, 593, 594] South Korea participates in the Chip 4 Alliance with the United States, Japan, and Taiwan to secure semiconductor supply chains and reduce reliance on China. The government also signed an MOU with ARM (i.e., British chip giant) to establish an "ARM School" that will train 1,400 semiconductor design specialists, addressing talent gaps in fabless and system-chip sectors. This partnership complements South Korea's broader workforce development strategy to cultivate 150,000 semiconductor professionals by 2031 through graduate programs, industry-academic partnerships, and global training tracks. Its partnership with TSMC, OpenAI, and other key companies reflects a strategic pivot toward AI-driven chip technologies.[595]

– The ARM School initiative (2026–2030) will support master's and doctoral programs, industry internships, and joint research projects at leading universities. South Korea currently has joint R&D programs with institutions like Korea Advanced Institute of Science & Technology (KAIST) and Tokyo University to accelerate innovation in semiconductors and lithography. KAIST operates advanced semiconductor programs and collaborates with Samsung and SK hynix through initiatives that provide full scholarships and guaranteed employment for graduates; joint research centers focus on next-generation memory and AI chip technologies. Samsung Electronics has also partnered with seven universities to offer integrated semiconductor courses combining undergraduate and graduate studies, internships, and guaranteed job placement. In addition, the Ministry of Science and ICT runs overseas training programs for AI semiconductor specialists at top universities such as Carnegie Mellon, University of Toronto, and Oxford, sending 120 graduate students annually for advanced coursework and research.

Manufacturing Leadership and Infrastructure: [596, 597, 598] South Korea accounts for more than 60% of the global memory semiconductor market (including DRAM and NAND flash). Samsung Electronics and SK hynix are major industry leaders; Samsung's Pyeongtaek Campus is recognized as the world's largest semiconductor facility; SK hynix leads in HBM for AI applications. Samsung also announced a $310 billion investment plan over a 5-year period to build new fabs for AI chips and memory, create an AI data center with 50,000+ NVIDIA GPUs, and generate 60K+ high-tech jobs. SK hynix is expanding its Yongin Semiconductor Cluster; the Center is backed by Korea's National Growth Fund and prioritizes AI semiconductor and deep-tech manufacturing capacity.

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National strategy and semiconductor investments

K-Semiconductor Strategy & K-Chips Act: [599, 600, 601] South Korea's K-Semiconductor Strategy is reinforced by the country's K-Chips Act and seeks to establish the world's largest semiconductor cluster and secure "super-gap" technologies by 2030. The plan includes tax incentives, infrastructure support, and deregulation aligned with global standards. A key component is the *Semiconductor Future Technology Roadmap*: a 10-year blueprint to guide R&D priorities and standards development. The strategy also emphasizes bilateral cooperation with ANSI and NIST to harmonize standards globally.

National Semiconductor Strategy 2030: [602] South Korea launched its National Semiconductor Strategy 2030 in 2024 to expand domestic chip production and research. The strategy pledged 620 trillion (~$450 billion USD) in combined public and private investments. The strategy designates semiconductors as a "national security sector" that provides tax incentives, infrastructure supports, and research grants to accelerate innovation in advanced logic, high-bandwidth memory, power management ICs, next-generation power semiconductors, neutral processing units (NPUs), and AI chips.

Semiconductor Ecosystem Support Package: [603] In addition to its National Semiconductor Strategy, South Korea also announced a Semiconductor Ecosystem Support Package worth 26 trillion (~$17.7 billion USD), which provides financial and infrastructure support for advanced semiconductors.

Semiconductor Future Technology Roadmap:[604] South Korea's roadmap outlines a 10-year plan to support the development and commercialization of 45 core technologies. The roadmap concentrates on building national capabilities across 45 core technologies grouped into three domains: new memory and next-generation devices; original semiconductor design technologies for AI, 6G, power, and automotive applications; and advanced process technologies for ultra-micronization and heterogeneous packaging. It promotes collaboration among industry, academia, and government through a dedicated public-private group and aligns domestic R&D with international standards efforts, referencing IEEE's IRDS roadmap. This strategic framework aims to position Korea as a global leader in semiconductor innovation while ensuring interoperability and supply chain resilience.

Standards development role: [605, 606, 607] The Korean Agency for Technology and Standards (KATS) plans to develop 39 new international semiconductor standards by 2031; at least 15 of these standards are targeted for completion by 2027. The standards cover wafer bonding reliability and power semiconductor wafer dicing precision. KATS collaborates with IEC, SEMI, and JEDEC and has signed MOUs with ANSI and NIST to strengthen bilateral cooperation. KATS harmonizes Korean Industrial Standards (KS) with ISO and IEC norms and promotes a market-driven, bottom-up approach through Co-operating Organizations for Standards Development (COSDs).

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Taiwan

Infrastructure and talent concentration: [608, 609, 610] Taiwan is home to Hsinchu Science Park—a globally recognized hub that hosts over 600 companies and 160,000 employees. The park integrates R&D, manufacturing, and academic collaboration, and is supported by leading universities and research institutes.[611] Taiwan is also addressing talent shortages through initiatives such as the Deep Cultivation Park Project and international semiconductor programs, which link students to internships and careers at companies like TSMC and United Microelectronics Corporation (UMC).

Innovation ecosystem and technology leadership: [612, 613, 614, 615] Taiwan is the world's top producer of advanced chips used in smartphones, data centers, and AI systems. Its companies are highly proficient at making extremely small and powerful chips for modern computing. They are supported by a dense network of science parks, research institutes, and universities that work closely with industry to develop new manufacturing techniques and packaging technologies.

International partnerships: [616, 617, 618, 619, 620] Taiwan's semiconductor industry has deep partnerships with major economies to secure supply chains and expand global capacity. TSMC has invested heavily in overseas fabs, including multi-billion-dollar facilities in Arizona (U.S.), Kumamoto (Japan), and Dresden (Germany), which are supported by their host governments. Taiwan's overseas facilities are meant to diversify production, reduce geopolitical risk, and reinforce its role as a trusted technology partner. Taiwan also seeks closer economic and technology ties with the EU. They engage in multilateral forums such as the Government/Authorities Meeting on Semiconductors (GAMS) and the World Semiconductor Council (WSC) to promote standards harmonization and policy coordination with the United States, EU, and Japan.

Role in standards and security: [621, 622, 623] Taiwan is highly active in global semiconductor standards development through SEMI, JEDEC, and its domestic association, Taiwan Semiconductor Industry Association (TSIA). TSIA coordinates Taiwan's participation in international standards-setting activities; this includes the World Semiconductor Council (WSC), JEDEC, and SEMI events. Taiwan also promotes cybersecurity standards for semiconductor equipment, such as SEMI E187, which sets specifications for fab equipment security.

Strategic industrial model and policy: [624, 625, 626, 627, 628] Taiwan built its leadership by focusing on a specialized business model: contract chip manufacturing for global customers. The approach was pioneered by TSMC, and it allowed companies worldwide to design chips while relying on Taiwan for production. Taiwan has spent decades investing and planning through the Industrial Technology Research Institute (ITRI), which created a strong foundation for today's ecosystem.

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Taiwan Semiconductor Strategic Policy 2025:[629, 630] Taiwan's 2025 Semiconductor Policy focuses on securing technological sovereignty and reinforcing its leadership in advanced chip manufacturing. It focuses on distributed manufacturing hubs, dual-use chip facilities, mandatory cybersecurity certification at the design level, sustained R&D investment incentives for cutting-edge process nodes, and programs for attracting and retaining top international semiconductor talent. The strategy promotes international standards harmonization through the Silicon Defense Pact, which seeks to enable mutual recognition of chip quality and security standards with allies such as the United States, Japan, and EU.

INDUSTRY CONSORTIA OR PUBLIC-PRIVATE PARTNERSHIPS

Compute Express Link (CXL) Consortium:[631, 632, 633, 634, 635, 636, 637, 638]

- CXL Consortium is an open industry group formed in 2019 by major tech companies to standardize high-speed, cache-coherent CPU-to-device and CPU-to-memory interconnects. CXL builds on PCIe (PCI Express) and adds protocols for low-latency memory sharing between CPUs and accelerators.
- The timeline of CXL specification releases is: CXL 1.0 in March 2019; 1.1 (June 2019); 2.0 (November 2020); 3.0 (August 2022); 3.2 (December 2024), and now 4.0 (November 2025). The latest spec increases bandwidth, supports bundled ports, adds memory Reliability, Availability, and Serviceability (RAS) enhancements, and enables full backward compatibility.
- CXL absorbed another consortium in 2022—Gen-Z—with the purpose of developing a single specification to advance interconnect technology and eliminate the risk of duplicated efforts going forward.
- The consortium offers compliance testing programs and hosts technical demos and educational sessions, including live demonstrations of CXL 4.0 and memory pooling at Supercomputing 2025 (SC'25).
- CXL addresses key data-center bottlenecks by enabling coherent memory pooling and resource sharing, accelerating AI/ML workloads, cloud services, and HPC applications through reduced latency and enhanced throughput.
- The consortium has approximately 200 member companies or more and has quickly become a "de facto standard" for next-generation data center architectures; CXL has been described as an "Industry Open Standard" that is "revolutionizing" and is the "Key to Next-Gen Server Architecture" for data centers.

Defense Advanced Research Projects Agency (DARPA) Joint University Microelectronics Program 2.0 (JUMP 2.0):[639, 640, 641, 642] JUMP 2.0 is a public–private research program launched in 2023 by DARPA and Semiconductor Research Corporation (SRC) to drive long-range innovations in microelectronics

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through university-led research centers. JUMP 2.0 builds on decades of DARPA–SRC collaboration and focuses on foundational advances for information and communication technologies (ICT) with an 8–12-year horizon. JUMP 2.0 is one of the key, long-term research efforts within DARPA's overarching, multi-billion-dollar program: the Electronics Resurgence Initiative (ERI). DARPA's JUMP 2.0 provides support to seven university-led centers whose research areas partly include AI system architectures, intelligent sensing, distributed compute fabrics, advanced packaging, and memory/storage technologies. Through SRC, the JUMP 2.0 program also funds undergraduate research experiences to broaden participation in semiconductor R&D. The Department of the Navy states that the JUMP 2.0 public-private research program is intended to strengthen U.S. leadership in microelectronics and ensure a pipeline of talent and IP for defense and commercial sectors.

European Semicon Coalition: [643, 644, 645] The European Semicon Coalition is a strategic alliance of EU member states formed to strengthen Europe's semiconductor ecosystem through coordinated investments, research, and standards development. The coalition manages a collective fund of approximately €43 billion to support advanced pilot lines, HI, quantum chip research, and a pan-European design platform. It fosters collaboration among industry, academia, and governments to accelerate innovation, ensure interoperability, and build supply chain resilience. The coalition also promotes sustainability initiatives and workforce development programs to address talent shortages.

Interuniversity Microelectronics Centre (IMEC): [646, 647, 648, 649, 650] IMEC is an independent, non-profit nanoelectronics and digital tech R&D center in Belgium; globally, it has 6,500+ researchers and is known as the "chip lab of the world." IMEC collaborates with 600+ industry partners, 200+ universities, and governments to drive next-generation semiconductor technologies. IMEC operates a state-of-the-art 300 mm CMOS pilot line and cleanroom infrastructure to support research in materials, patterning, devices, packaging, photonics, sensing, and system scaling. It serves as a global R&D hub accelerating semiconductor innovation—from nano to system scales—through collaborative, vendor-neutral research, which helps to reduce duplication and speed up commercialization. IMEC offers open process design kits (PDKs) for advanced semiconductor nodes, enabling academic and industry partners to design and validate chips using IMEC's leading-edge process technologies without proprietary restrictions. This access is key for collaborative innovation and accelerated pre-commercial research. IMEC engages in public-funded projects under EU and national programs (e.g. EU Chips Act NanoIC line) and has signed strategic partnerships (e.g., with ASML and SCREEN).

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RISC-V International: [651, 652, 653, 654] RISC-V International is a global non-profit organization that manages the open RISC-V instruction set architecture (ISA).[655] Most ISAs are proprietary; RISC-V is royalty-free and enables anyone to design processors without licensing fees. RISC-V uses member-driven technical working groups to oversee and openly publish specifications for ISAs and ISA extensions for features like vector processing and security. The organization comprises 4,500 member organizations globally, including semiconductor companies, cloud/cloud-native providers, universities, open-source toolchains, and end-market segments. Members include Intel, NVIDIA, Alibaba, Qualcomm, SiFive, and Espressif. RISC-V hosts global events such as the RISC-V Summit to share updates, showcase implementations, and encourage collaboration across hardware and software communities. RISC-V's open ISA is gaining widespread adoption across sectors including AI, automotive, IoT, and edge computing; companies and research groups use the open ISA to design processors tailored for diverse applications. The open ISA is helping to lower barriers to innovation and reduce reliance on proprietary architectures. Analysts say the demand for AI and embedded systems is driving the integration of RISC-V cores into an estimated over 60 billion devices by 2027.

SEMI Semiconductor Manufacturing Cybersecurity Consortium (SMCC): [656, 657, 658, 659]

In September 2024, SEMI launched the SMCC as a public–private partnership to adapt the broad requirements of the NIST Cybersecurity Framework 2.0 into a set of highly specific and actionable security controls tailored to semiconductor manufacturing environments. The SMCC collaborated with NIST's National Cybersecurity Center of Excellence (NCCoE) to release the draft "Community Profile" in early 2025 and hosted workshops to gather industry feedback from fabrication facilities, equipment vendors, and supply chain participants.

The collaboration created a semiconductor-specific cybersecurity profile defined by correlating the NIST Framework's security functions with the core operational objectives of manufacturing (e.g., maximizing yield and tool uptime). This profile leverages SEMI standards, such as SEMI E187, to implement specific controls for authenticated access and hardened equipment configurations. This ensures supply chain resilience and aligns with national critical-infrastructure security requirements.

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Universal Chiplet Interconnect Express (UCIe) Consortium: [660, 661, 662, 663, 664]
The UCIe Consortium is an industry alliance that formed in March 2022; it defined a common, shared standard for connecting chip segments (chiplets) (i.e., UCI 1.0). This standard enables interoperable multi-die systems across 2D/2.5D and 3D/hybrid-bonded packages; successive releases (e.g., UCIe 2.0 and UCIe 3.0) expand scope to testability, manageability, security, and higher data rates.

UCIe has several working groups: electrical, protocol, form factor & compliance, manageability/security, and systems & software. These groups establish standards and protocols for conformance, discovery, power/thermal management, error reporting, and debug architectures so chiplets from different vendors can be reliably mixed and matched. The UCIe 2.0 spec update added 3D stacking support optimized for hybrid bonding. Later, the UCIe 3.0 specification doubled bandwidth for 2D chiplets and broadened ecosystem adoption through compliance tooling and partner development.

According to the AMD Chiplet Ecosystem Whitepaper, UCIe's contribution to standardizing die-to-die interconnects for chiplets across packing options lowers integration risk, enables best-of-breed chiplet ecosystems, and shortens time-to-market for heterogeneous systems.

UCIe chiplet interconnects are evolving toward 3D interconnects (with shrinking bump pitches and hybrid bonding); these changes will address power, bandwidth density, and latency, which are considered key bottlenecks for next-generation AI and HPC.

Membership at the UCIe is also growing; the membership comprises foundries, OSATs, EDA vendors, and system integrators, which may indicate greater industry alignment around interoperability and compliance frameworks.

U.S. FEDERAL ROLES

This subsection summarizes how key U.S. federal agencies, bureaus, and offices are driving semiconductor and microelectronics standardization through technical leadership, policy frameworks, and strategic investments. It highlights the distinct roles of U.S. federal agencies in shaping standards priorities, funding pre-standardization research, and coordinating interagency efforts under initiatives like the CHIPS and Science Act. These activities ensure interoperability, security, and sustainability across the semiconductor lifecycle while reinforcing U.S. competitiveness and resilience in global supply chains.

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Bureau of Industry and Security (BIS)

Key Role
Enforces export controls to restrict access to advanced semiconductors and manufacturing equipment and safeguard U.S. technological leadership and national security [665, 666]

Contributions
Administers the Export Administration Regulations (EAR), which govern the export, reexport, and transfer of advanced semiconductors and manufacturing equipment to protect U.S. national security and foreign policy interests [667, 668]

Sets performance-based criteria (e.g., logic chip density, interconnect pitch, equipment capabilities) in EAR updates, which influence design and manufacturing standards for compliance [669, 670]

Provides licensing procedures and due diligence requirements for companies exporting chips, equipment, and related technologies to restricted destinations

Maintains lists of organizations (i.e., "Entity List") subject to trade restrictions to prevent unauthorized access to advanced semiconductor technologies, supporting global security and compliance standards[671]

National Aeronautics and Space Administration (NASA)

Key Role
Develops and applies semiconductor standards for space systems and avionics

Contributions
Advances semiconductor research for extreme environments (e.g., silicon carbide [SiC] electronics capable of operating at 500–650°C); NASA Glenn's work informs design rules and reliability standards for high-temperature semiconductors used in aerospace and energy sectors [672, 673]

Develops and maintains standards for high-reliability microelectronics packaging and interconnects for space applications; publishes roadmaps and technical guidelines addressing thermal stress, electromigration, and advanced packaging reliability to inform aerospace and semiconductor standards [674]

Explores microgravity manufacturing of semiconductors through In Space Production Applications (InSPA); NASA studies crystal growth and defect reduction in low Earth orbit to establish process guidelines that could influence future semiconductor fabrication standards [675, 676]

Operates the NASA Electronic Parts and Packaging (NEPP) Program, which evaluates advanced semiconductor devices and packaging technologies for reliability; NEPP's work establishes NASA's internal mandatory standards for space-grade electronics;[677] the NEPP program also informs external voluntary consensus standards through active participation in bodies like JEDEC and

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SAE, and develops qualification guidelines that are often mandated for U.S. government-procured aerospace microelectronics [678]

Participates in JEDEC and SAE standards committees through the NASA Electronic Parts Assurance Group (NEPAG); contributes to defining qualification requirements for complex microcircuits (e.g., Class Y ceramic-based non-hermetic devices) and packaging integrity test plans [679, 680]

Publishes NASA-STD-8739 series for Electrical, Electronic, and Electromechanical (EEE) parts assurance, including selection, screening, and derating standards; these documents set rigorous criteria for microelectronics reliability and influence broader aerospace standards. [681, 682]

National Institute of Standards and Technology (NIST)

Key Role
Leads federal agency for semiconductor and microelectronics standards development, metrology, and CHIPS Act implementation

Contributions
Administers the **CHIPS for America R&D programs,** including the NSTC and Advanced Packaging Manufacturing Program, which integrate standards development into R&D and manufacturing initiatives [683]

Chairs the Semiconductors and Microelectronics Standards Working Group (SMSWG) under the Interagency Committee on Standards Policy (ICSP), aligning federal priorities with the National Standards Strategy for Critical and Emerging Technologies [684]

– Coordinates cross-agency identification of semiconductor standards focus areas, priority topics, and gaps; NIST's work with SMSWG has culminated in an annual report (NIST IR 8577) that provides strategic recommendations to the ICSP on key Federal standards efforts [685, 686]

Convenes the semiconductor standards community through summits and workshops to develop an ecosystem-wide roadmap to identify standards priorities [687]

Coordinates supply chain security standards through interagency agreements, aligns CHIPS investments with dense requirements and trusted sourcing criteria to mitigate risks in semiconductor procurement [688, 689]

Coordinates U.S. participation in ISO/IEC and IEEE semiconductor standards committees [690, 691, 692]

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Develops **measurement science and metrology standards** for semiconductor devices, advanced packaging, and reliability testing; sponsors workshops on semiconductor metrology challenges to inform standards priorities [693, 694]

I**mplemented the CHIPS and Science Act,** allocating $50 billion for semiconductor manufacturing and $11 billion for R&D; includes standards-related programs under NIST to strengthen U.S. leadership in metrology, interoperability, and secure manufacturing practices [695, 696]

Launched CHIPS Metrology Program to advance measurements science and metrology standards for next-generation semiconductor manufacturing; supports development of reference materials and calibration protocols for high-density packaging and chiplet integration [697, 698]

Leads development of **documentary standards for semiconductor metrology and assurance** through CHIPS R&D initiatives [699, 700]

Promotes international standards engagement through bilateral and multilateral forums to harmonize semiconductor standards globally [701, 702]

Publishes annual reports identifying strategic standards focus areas (e.g., advanced packaging, HI, cybersecurity for microelectronics); **identifies gaps requiring pre-standardization R&D** [703, 704]

National Science Foundation (NSF)

Key Role
Funds fundamental semiconductor research and workforce development; invests in programs that advance secure, interoperable, and energy-efficiency semiconductor technologies while supporting education and training initiatives to build a skilled workforce in microelectronics manufacturing and design; NSF programs emphasize co-design approaches and curriculum development aligned with industry standards [705, 706, 707]

Contributions
Aligns broader CHIPS Act implementation with research and workforce standards, including authorization for NSF programs that codify Technology, Innovation & Partnerships (TIP) and designate $200 million specifically for semiconductor workforce training and education [708, 709]

Backs evidence-based technician and educator training programs, including Transformative Approaches to Educating the Semiconductor Workforce (TA-ESW) and ETA-ESW (Micron partnership); these efforts formalize learning outcomes and lab competencies (e.g., lithography steps, contamination control, measurement traceability) that reflect standards in manufacturing settings [710, 711]

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Creates public–private pathways to "standards-aware" curricula and credentialing—for example, NSF + Intel invested $7.6 million (2024) in six projects to modernize technician education and S-STEM scholarships, which helped two- and four-year institutions align program outcomes with industry expectations for yield, reliability, process control, contamination control, cleanroom operation, equipment maintenance, and metrology proficiency [712, 713]

Expands fundamental research on secure, interoperable semiconductor systems; NSF supports co-design methods (materials/devices /circuits/ architectures) and access to shared fabrication/test facilities that help translate research into repeatable, standards-aligned practices for energy efficiency, security, and reliability [714, 715]

Invests in Future of Semiconductors (FuSe) programs, addressing challenges in energy efficiency, performance speed and capacity, process sustainability, robustness, cost-effectiveness, interoperability, and secure design—aligned with CHIPS Act goals; awarded $45.6 million in 2023 and $42.4 million in 2024 to advance domain-specific computing, hetero-integration, and beyond-CMOS materials; these areas feed into design rules, process sustainability guidelines (for materials recyclability and environmental impact), metrology baselines (e.g., for novel materials and intrinsic performance limits), and interoperability expectations [716, 717]

Partnered with NIST to create the workforce initiative: the National Network for Microelectronics Education (NNME); NNME provided $30 million to produce consistent, rigorous curricula, instructional materials, and hands-on modules; NNME helps ensure standards literacy in workforce training; outcomes of the NNME workforce initiative are aligned with industry norms for cleanroom safety, process control, and device characterization [718, 719, 720, 721, 722]

U.S. Department of Defense (DoD)

Key Role

Secures defense microelectronics through quantifiable assurance frameworks; sets procurement requirements and influences standards for hardware assurance, supply chain security, and lifecycle risk management [723, 724]

Contributions

Adopted quantifiable assurance frameworks to replace the legacy Trusted Foundry model; influences standards for hardware assurance, supply chain integrity, and lifecycle security for defense microelectronics [725, 726]

Defines levels of hardware assurance and lifecycle risk management guidance for defense microelectronics, providing criteria that inform acquisition practices and industry standards [727, 728]

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Establishes supply chain security standards under National Defense Authorization Act (NDAA) mandates for trusted microelectronics procurement, including requirements for supplier vetting and operational security [729, 730]

Funds and manages Microelectronics Commons under the CHIPS Act to accelerate secure domestic manufacturing, prototyping, and workforce development aligned with defense standards [731, 732]

Publishes technical guidance for Field-Programmable Gate Array (FPGA) security and hardware assurance to inform standards for defense-grade microelectronics [733]

U.S. Department of Energy (DOE)

Key Role
Advances semiconductor R&D for energy efficiency and HPC; supports standards for sustainable microelectronics [734, 735]

Contributions
Advances WBG semiconductor standards through PowerAmerica Institute; focus is on high-performance, energy-efficient power electronics for electrification and grid integration; DOE also helps develop commercialization guidelines and workforce training aligned with manufacturing standards [736, 737]

Coordinates national lab R&D for ultra-energy-efficient devices via the EES2 roadmap and lab calls, targeting more than 10-x improvements in transistor-level efficiency and influencing future device-level performance benchmarks [738, 739]

Established Microelectronics Science Research Centers (MSRCs) under the CHIPS and Science Act to advance fundamental research in energy-efficient and extreme-environment semiconductors; the Centers develop early-stage standards for materials, device design, and manufacturing science [740, 741, 742]

Leads supply chain security and resilience assessments for semiconductors under Executive Order 14017, publishing DOE's Semiconductor Supply Chain Deep Dive Assessment with recommendations that influence standards for domestic manufacturing and secure sourcing [743, 744]

Leads the Energy Efficiency Scaling for Two Decades (EES2) Initiative, which includes roadmap development for semiconductor energy efficiency standards [745]

Participates in the CHIPS-funded SMART USA Institute for digital twin technology to standardize advanced semiconductor manufacturing processes [746]

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White House Office of Science and Technology Policy (OSTP)

Key Role
Coordinates interagency semiconductor standards policy and research strategy; chairs the National Science and Technology Council (NSTC) and its Subcommittee on Microelectronics Leadership to align federal priorities for microelectronics R&D; ensures standards development supports U.S. competitiveness, national security, and economic growth [747, 748]

Contributions
Coordinates interagency implementation of the National Strategy on Microelectronics Research; the strategy embeds standards priorities for advanced packaging, heterogeneous integration, and secure supply chains into federal R&D plans; OSTP provides strategic guidance through the NSTC Subcommittee on Microelectronics Leadership (SML) [749, 750]

Integrates semiconductor standards into cross-cutting federal initiatives; this includes the National Standards Strategy for Critical and Emerging Technologies; OSTP promotes alignment of U.S. positions in international standards bodies to strengthen global competitiveness [751, 752]

Issues guidance on scientific integrity and reproducibility standards through initiatives like the Gold Standard Science directive; reinforces transparency and rigor in federally funded semiconductor R&D, which underpins credible standards development [753, 754]

Operates the National Semiconductor Technology Center (NSTC) Subcommittee on Microelectronics Leadership (SML) to coordinate U.S. federal efforts in microelectronics research, development, and supply chain security; convenes interagency working groups and collaborates with industry consortia to align federal investments with standards development, ensuring U.S. leadership in global semiconductor ecosystems and alignment with technical standards work by NIST, IEEE, SEMI, and ISO/IEC [755, 756, 757, 758]

Provides policy leadership for CHIPS Act implementation across agencies and sets common priorities for standards development in metrology, advanced manufacturing, and supply chain security; works with OMB and technical agencies to ensure consistency with national security and economic goals [759, 760]

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Opportunities/ Recommendations

This section identifies actionable opportunities for advancing semiconductor and microelectronics standardization, based on the findings of this environmental scan. The recommendations draw from observed gaps, emerging needs, and stakeholder priorities identified throughout the report, including insights from government strategies, industry roadmaps, and academic research. These opportunities are intended to guide future planning, support strategic engagement, and reinforce ASTM's role in shaping effective standards that promote interoperability, reliability, and innovation across the semiconductor ecosystem.

Advance standards for chiplet interoperability: [761, 762, 763, 764, 765, 766] Chiplet-based architectures are reshaping semiconductor design, but standards remain narrowly focused on physical interconnects like UCIe. Industry requires frameworks that extend beyond the physical layer (PHY) to include system-level protocols for lifecycle management, security, and DFx (testability, manageability, debug) to help improve interoperability across vendors. Without these standards, integration risk and design complexity will continue to slow adoption of heterogeneous packaging. Initiatives such as JEDEC's JEP30 and the Open Compute Project's chiplet design kits offer early guidance, but they lack formal compliance and certification pathways as needed for global scale-up.

Advance standards for power materials (SiC and GaN) device testing, reliability, and interoperability: [767, 768, 769, 770] WBG semiconductors such as silicon carbide (SiC) and gallium nitride (GaN) enable higher voltage, temperature, and efficiency performance for EVs, power electronics, and RF systems. JEDEC's JC-70 committees have introduced baseline standards for dynamic testing and reliability (e.g., gate charge, switching, reverse recovery); however, gaps remain in accelerated lifetime testing, thermal-mechanical stress, and board-level integration. IEC and IEEE initiatives call for harmonized qualification criteria and standardized interfaces to ensure interoperability across suppliers and system designs. This would help reduce design risks, improve supply chain consistency, and accelerate adoption in applications like automotive, aerospace, and renewable energy.

Define protocols to validate AI-driven chip design for trust and reproducibility: [771, 772, 773, 774, 775] AI-driven EDA platforms [776] are enabling dramatic gains in productivity, testbench generation, coverage acceleration, and PPA (performance, power, area) in chip design. Ensuring consistent and trustworthy adoption across the industry requires new standards that specify model performance benchmarks, coverage metrics, explainability requirements, human-in-the-loop verification checkpoints, and bias/method validation. These standards can be based on frameworks like NIST's AI test, evaluation, validation and verification (TEVV) and IEEE's AI trust assessment specs for rigorous system-level validation; they would enable reproducible design results, reduce flow variability EDA tools and fabs, and support certification of AI-generated layouts and verification artifacts (i.e., for compliance and cross-vendor interoperability).

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Develop reliability and thermal frameworks for 3D packaging: [777, 778, 779] Advanced packaging technologies such as 2.5D and 3D integration introduce reliability challenges that traditional standards do not address (e.g., issues like micro-bump fatigue, TSV stress, and heat dissipation across stacked dies). These risks are particularly critical for AI and HPC systems, where thermal limits can directly impact performance and yield. Industry roadmaps emphasize the need for shared frameworks covering stress testing, thermal modeling, PHM (prognostics and health monitoring) building blocks, board-level attach requirements, SiP design kit and data format standardization, and co-design practices. Establishing standards for these needs will help manufacturers reduce costly failures and accelerate adoption of advanced packaging in mission-critical applications.

Expand security standards to cover fab equipment, digital twins, and cloud-connected workflows: [780, 781, 782, 783, 784, 785] Traditional IT frameworks are not adequate for highly automated fabs with thousands of tools exchanging data with predictive maintenance systems and cloud analytics. SEMI's E187 and E188 standards already define baseline requirements for equipment cybersecurity (i.e., for OS hardening, authentication, malware scanning, and event logging) but their adoption is lacking. Standards must address secure data flows, encryption for machine-to-cloud connections, and integrity checks for virtual models as fabrication facilities deploy digital twin models and AI-driven optimization. NIST's Semiconductor Manufacturing Cybersecurity Profile (IR 8546) complements these efforts by adapting the Cybersecurity Framework (CSF) for fab-specific risks, which would thereby enable harmonized protocols that protect both physical assets and digital ecosystems.

Harmonize metrics for energy, water, emissions, and material reuse across fab equipment and product life cycles: [786, 787, 788, 789, 790, 791, 792, 793, 794, 795, 796, 797, 798, 799] SEMI S23 provides repeatable methods to measure equipment energy and utilities, which are key inputs for fab-level product carbon footprint (PCF) baselines. SCC's value-chain analysis calls for harmonized methodologies and transparent data for Scope 1–3 emissions; The U.S. Environmental Protection Agency (EPA) Sustainable Materials Management (SMM) and EU's Circular Economy/Digital Product Passport frameworks push life-cycle reporting and standardized product data fields. Water usage remains a critical lever: fabs face rising ultrapure water (UPW) demand and evaporative losses. NIST and SEMI roadmaps indicate efficiency metrics (e.g., gallons per wafer, reuse ratios) are a near-term standards priority to link shop-floor measurements with interoperable lifecycle analysis artifacts.

Strengthen supply chain traceability and provenance: [800, 801, 802] Semiconductor supply chains are increasingly vulnerable to risks such as counterfeiting, tampering, and unauthorized component substitution. Standards for digital chip passports and secure serialization can provide end-to-end visibility and help ensure components are authentic and traceable from wafer fabrication through final assembly. Emerging approaches—such as blockchain-enabled traceability and hardware

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roots of trust—align with secure-by-design mandates in the CHIPS Act and EU Chips Act. These standards will strengthen global supply chain integrity, support export control verification, and build confidence in multi-vendor ecosystems.

Use shared testbeds to align standards and reduce regional fragmentation:[803, 804, 805, 806, 807, 808, 809] Several major standards bodies increasingly recognize the value of collaborative "sandbox" environments where draft specifications can be tested before formal adoption. These pre-standardization testbeds often leverage digital twin models and allow stakeholders to validate interoperability, performance metrics, and security protocols under real-world conditions. This approach supports "co-opetition" across regions and helps reconcile differences between frameworks like the U.S. CHIPS Act and EU Chips Act, accelerating consensus and reducing costly duplication in semiconductor manufacturing standards.

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